1435/1435-83 HIGH FREQUENCY FAST SETTLING OPERATIONAL AMPLIFIER

The 1435/1435-83 is an Ultra-Fast Differential Input Operational Amplifier designed for the precision amplification of wide band complex waveforms with frequency components from DC to one Gigahertz. By precision is meant gain accuracies of 0.01%. This is reflected in the settling time specification of 70 nanoseconds to 0.01% for a 10 volt output step.

Such performance is made possible by a unique design with high open loop gain, flat frequency response beyond 100 kHz and smooth 6 dB/octave rolloff beyond 100 MHz (see Bode plot, Fig. 1). When handling complex waveforms such as square pulses, overshoot is less than 1% of output pulse amplitude.

Applications for the 1435/1435-83 are based on using the precision capabilities of the basic differential input op amp at frequencies higher than ever before possible. These include 20 to 40 dB gain differential input video mixers with 0.1% gain stability; peak detectors (and sample & holds) which can capture 25 nanosecond pulses to 1% accuracy and 70 nanosecond pulses to 0.01% accuracy; Video A to D Converters and DAC's; and sub-microsecond precision analog comparators.

FEATURES

- Mil Std 883 Processing (1435-83)
- Gigahertz Gain Bandwidth Product
- 70 nsec Settling to 0.01%
- CMRR 60 dB @ 1 MHz
- −55°C to +125°C Operation

APPLICATIONS

- Radar & Sonar Signal Processing
- Microwave Transmitter Modulators
- Graphic CRT Displays
- Linear Video Mixers
- Video ADC, DAC, S-H

MIL STD 883 PROCESSING

The 1435-83 is processed to MIL STD 883, including Temperature Cycling and 168 hours of Burn In (see table, page 4). The 1435 has the same processing less Temperature Cycling and Burn In.

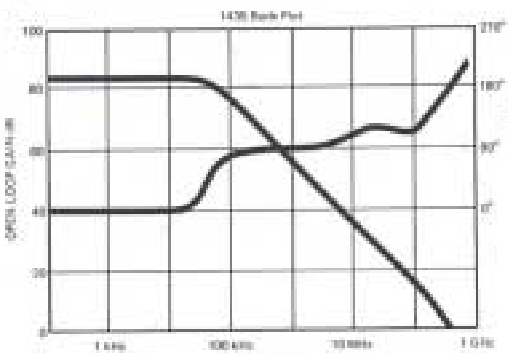


Figure 1. Open Loop Gain and Phase vs. Frequency

BASIC CONNECTIONS & WIRING TECHNIQUES

Figure 2 illustrates the basic connections required for the 1435 in schematic form and with a suggested physical layout. The layout is shown to illustrate the wiring techniques required to obtain the specified high frequency/time response from the 1435. The circuit should be built on a ground plane with minimum length point to point connections directly to amplifier pins. If a socket is necessary, it should be of Teflon such as the Augat Model 114-AG-2A. Remember, 1000 ohms and 10 pF provides a time constant of 10 nsec.

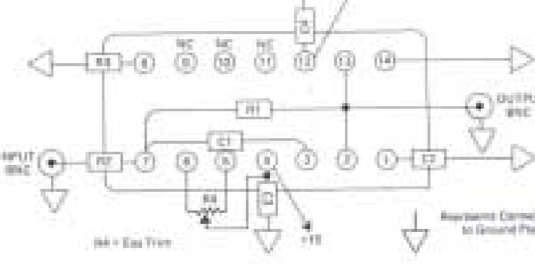


Figure 2A. Suggested Layout

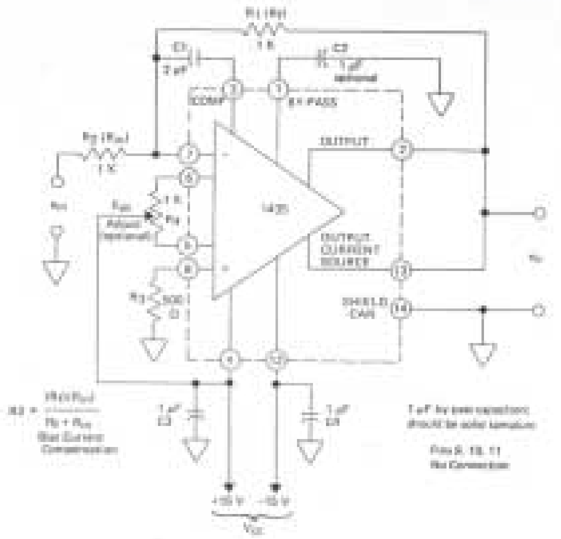


Figure 2B. Schematic

Note should be taken in using the output circuit of the 1435 to make sure that for most applications pins 2 and 13 are connected together. When using a booster as in Figure 5 they are not connected together.

Stability and Compensation

Shown as a circuit gain of one inverter in Figure 2, the 1435 operates in any of the conventional op amp circuits including the Follower, Current to Voltage Converter, Integrator, etc. However, it must be used at a "noise gain" of at least 2. (Noise Gain = 1 + R_f/R_{IN}). That is, it can operate as a gain of one inverter or differential amplifier, but as a follower it must operate with a gain of at least 2 (see Figure 3). As an I to V it must also be "noise gained" (see Figure 4).

Capacitor C1 in Figure 2 is a 2 pF compensation device and must be used when the noise gain is less than 10 for stable operation.

R3, the resistor connected to pin 8, the + input, provides compensation for bias current. Its value should be that of R_{IN} and R_f in parallel. The 1K Eos Trim or Balance Pot is optional. The 1 μF by-pass capacitor connected to pin 1 is required only when the feedback circuit is being switched electronically.

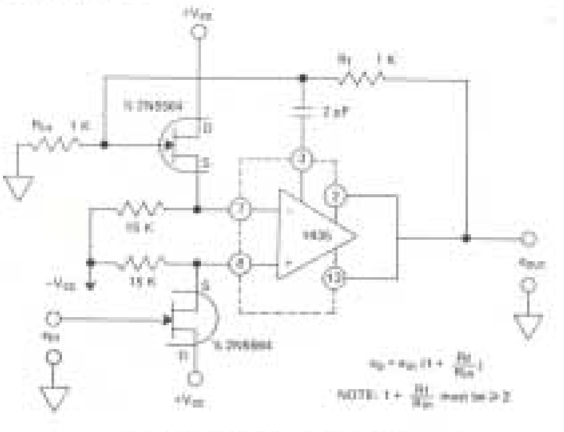


Figure 3. 1435/1435-83 as High Impedance Input Follower With Gain (shown with GAIN=2)

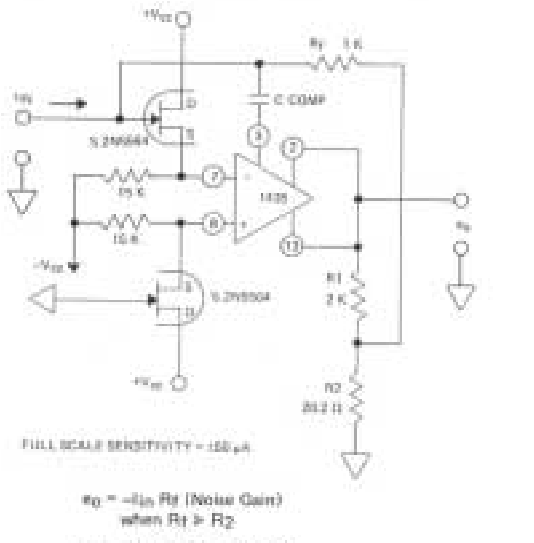
When operating at the low impedance required of the 1435, care should be taken to include the load provided by the feedback resistor in calculating the total output load of the amplifier.

Operation As A Follower

When operated as a follower, the 1435 must have a "noise gain" of at least 2. In addition, high common mode input impedance and low bias current are usually required. Figure 3 shows the 1435 connected as a "follower with gain of 2", (that is, $1 + \frac{R_f}{R_I} = 2$) with a dual FET as "Source Follower" connected to each input. These FET's raise input Z to thousands of megohms, and reduce bias current to hundreds of picoamps. Both more than sufficient for the impedances involved.

Operation As A Current to Voltage Converter

Like the Follower, Current to Voltage Converter operation requires low I_b, High Z, and "Noise Gain". These are obtained in the circuit of Figure 4, with FET's again providing the increase in impedance. The "Noise Gain" is provided by R1 and R2 per the equation $NG = 1 + \frac{R1}{R2}$. This provides the added advantage of making R_f, the current sensing resistor, "look" bigger than it is by the NG factor, but the stray capacity across it which lowers high frequency response sees the actual R_f. Thus the circuit of Figure 4 has a full scale sensitivity (±5 V e_0) for ±50 μA input.



$e_0 = -I_{in} R_f$ (Noise Gain)
when $R_f \gg R_2$

$e_0 = -I_{in} R_f (1 + R1/R2)$

$e_0 = -I_{in} R_f [1 + R_1/(R_2 + R_f)/(R_2 \cdot R_f)]$
for any value of R_f

Noise Gain must be ≥ 2
C Comp = 0 if Noise Gain ≥ 10

Figure 4. 1435/1435-83 as Fast Current to Voltage Converter

Operation As An Integrator

The 1435 is operated as an integrator by again adding FET's to the inputs and replacing R_f with a capacitor of up to 5 pF (for stable operation).

Operation With ±100 mA Output

When it is necessary to drive a load of less than 500 ohms with the full ±5 V 1435 output, the circuit of Figure 6 is used. This conventional booster will drive ±100 mA into 50 ohms in parallel with 70 pF and not oscillate. With a 10 pF load it will provide 0.01% settling in 100 nsec. Thus the 1435 can drive 50 Ω co-axial cable. This booster circuit can be used with the circuits of Figures 3 through 5 and at higher "noise gains".

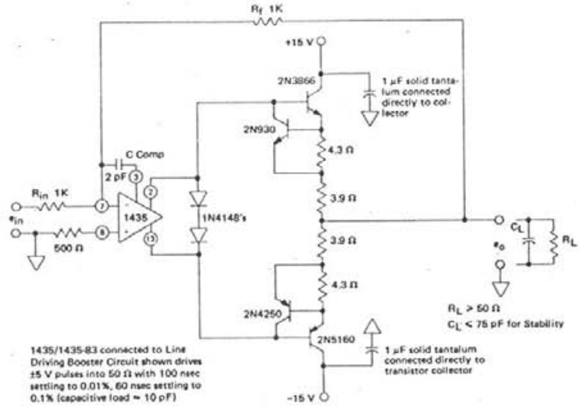


Figure 5. Booster

SETTLING TIME MEASUREMENT

The measurement of anything to one part in 10,000 (0.01%) requires care. The measurement of amplifier settling time of under 100 nanoseconds to that accuracy requires great care. Teledyne Philbrick measures 1435/1435-83 settling time in the circuit of Figure 6. The Settling Time Test Point or "settle point" is connected to an emitter follower buffer for 0.1% measurement and a gain of 5 buffer for 0.01%. For a detailed discussion of these measurement techniques, see TP Model 1430 data sheet.

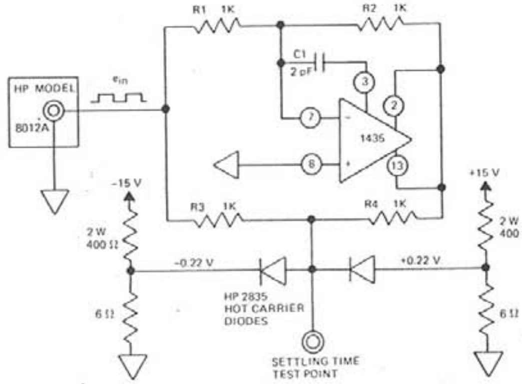


Figure 6. Test Circuit

SPECIFICATIONS

CMRR vs Frequency & Settling Time vs Noise Gain

In addition to Open Loop Gain vs Frequency (Figure 1) it is useful to have several other 1435 parameters as a function of frequency or time. Since a major application is as a high frequency differential amplifier, a plot of Common Mode Rejection vs. Frequency is provided in Figure 7. Figure 8 shows settling time vs noise gain to indicate performance up to a gain of 10 as an inverter or 11 as a follower.

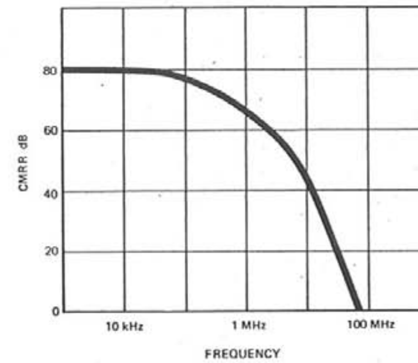


Figure 7. 1435/1435-83 CMRR vs. Frequency

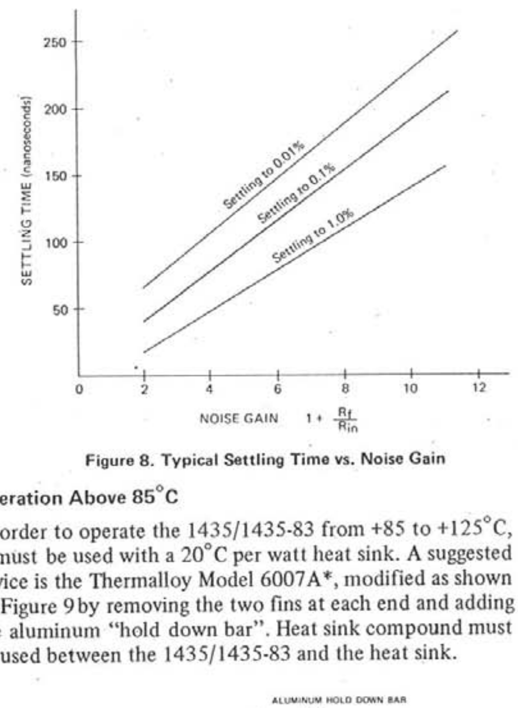


Figure 8. Typical Settling Time vs. Noise Gain

Operation Above 85°C

In order to operate the 1435/1435-83 from +85 to +125°C, it must be used with a 20°C per watt heat sink. A suggested device is the Thermalloy Model 6007A*, modified as shown in Figure 9 by removing the two fins at each end and adding the aluminum "hold down bar". Heat sink compound must be used between the 1435/1435-83 and the heat sink.

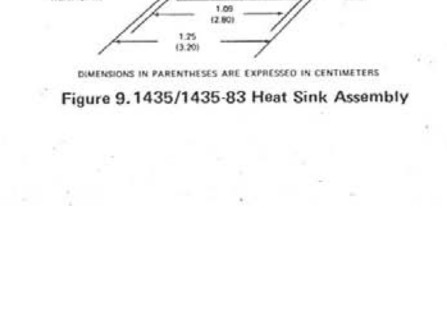


Figure 9. 1435/1435-83 Heat Sink Assembly

SPECIFICATIONS @ +25°C, V_{cc} = ±15 V, R_L = 500 Ω, unless otherwise indicated.

	TYPICAL	GUARANTEED
OUTPUT RANGE		
Voltage (Peak)	±7 V	±5 V
Current	±14 mA	±10 mA
VOLTAGE GAIN (dc Open Loop)		
Rated Load	85 dB	80 dB
FREQUENCY RESPONSE (Inverting and Non-Inverting) (1)		
Small Signal (Gain Bandwidth Product) (2)	1000 MHz	700 MHz
Small Signal (Unity Gain Open Loop)	500 MHz	----
Sine Wave Power Out, max.	10 MHz	8 MHz (C_1 = 0.5 pF)
Peak to Peak Out (Triangle Wave), max.	12 MHz	----
Capacitive Load without Oscillation, max. (NG ≥ 2)	----	1000 pF (C_1 = 3 pF)
TIME RESPONSE (Inverting and Non-Inverting) (1)		
Settling Time (3)		
10 V Step to within 2.5 mV (0.025%)	60 nsec	75 nsec (C_f = 1 pF)
10 V Step to within 1 mV (0.01%)	70 nsec	---- (C_f = 1 pF)
5 V Step to within 50 mV (1%)	25 nsec	----
5 mV (0.1%)	40 nsec	60 nsec
1 V Step to within 10 mV (1%)	10 nsec	----
1 mV (0.1%)	20 nsec	----
Slew Rate (1)	300 V/µsec	250 V/µsec (C_1 = 0.5 pF)
Overshoot, max.	1%	----
Propagation Delay	5 nsec	----
Rise Time (10 V step)	40 nsec	----
Overload Recovery Time	50 nsec	----
INPUT VOLTAGE RANGE/CMRR/IMPEDANCE		
Common Mode for dc Linear Operation	±11 V	±10 V
Common Mode Fault, absolute max.	----	$\pm V_{cc}$
Differential Between Inputs, max.	----	±2 V
Common Mode Rejection Ratio at dc	90 dB	80 dB
Common Mode Rejection Ratio at 1 MHz (4)	70 dB	----
Input Impedance at dc (Common Mode)	1 MΩ‖2 pF	----
Input Impedance at dc (Differential)	2.5 KΩ‖2 pF	----
INPUT OFFSET VOLTAGE		
Initial (without External Trim)	±2 mV	±5 mV
Zero Adjustment (optional)	----	1 KΩ pot
Vs. Temperature (Avg. −55°C to +125°C) (1435-83)	±5 µV/°C	±25 µV/°C
(Avg. −25°C to +85°C) (1435)	±5 µV/°C	±25 µV/°C
Vs. Power Supply (PSRR)	0.15 mV/VΔV_{cc}	----
INPUT BIAS CURRENT		
Initial (without External Trim)	10 µA	20 µA
Vs. Temperature (Avg. −55°C to +125°C) (1435-83)	----	100 nA/°C
(Avg. −25°C to +85°C) (1435)	----	100 nA/°C
NOISE (Referred to Input)		
Flicker (0.01 Hz to 10 Hz)		
Voltage (Peak to Peak)	15 µV	----
Current (Peak to Peak)	2.5 nA	----
Midband (100 Hz to 10 kHz)		
Voltage (rms)	1.6 µV	----
Current (rms)	2.5 nA	----
Wideband (10 Hz to 1 MHz)		
Voltage (rms)	5.2 µV	----
Current (rms)	3.5 nA	----
POWER REQUIREMENTS		
Nominal Supply Voltage	----	±15 V
Supply Voltage Range	±12 to ±16	----
Quiescent Current @ V_{cc} = ±15 V	----	±30 mA
TEMPERATURE RANGE		
Operating	----	−55°C to +85°C +125°C with 20°C/watt heat sink
Storage	----	−65°C to +150°C
MTBF (5) 1435-83	1.06/10^6 hours	

NOTES:

(1) Frequency Response and Slew Rate measurements made in circuit of Figure 2.
(2) Measured at 10 MHz
(3) Settling Time measured in circuit of Figure 6. See Figure 8 for plot of Settling Time vs. Noise Gain.
(4) See Figure 7 for plot of CMRR vs Frequency.
(5) Calculated per MIL Handbook 217B at 85°C.

RECOMMENDED POWER SUPPLIES: 2212 or 2403 or 2301.

SCREENING SIMILAR TO MIL-STD 883 METHOD 5008

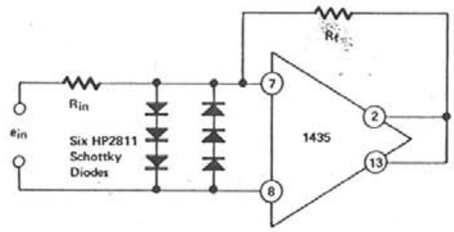
Test	Methods and Conditions	Purpose
*Internal Visual	Method 2017	Removes potentially defective units with respect to materials, construction, and workmanship.
*Stabilization Bake	Method 1008, Condition C 24 hours at 150°C	Preconditioning treatment to stabilize circuit components prior to conducting further testing and trimming.
*Constant Acceleration	Method 2001, Condition B Y_1 Axis, 10,000 g	Removes potential failures due to weak wire or chip bonding.
*Seal, Fine and Gross	Method 1014, Fine Leak Condition A & C Bomb time 1 hr. at 30 psi; Leak Rate $< 5 \times 10^{-7}$ cc/sec; Gross Leak, Condition C_1, no bubbles	Verifies Integrity of hermetic package
Burn In	Method 1015 Condition B 160 hours at 125°C	Reduces infant mortality rate
Temperature Cycling	Method 1010, Condition B 10 cycles from $-55°C^{+0°C}_{-5°C}$ to $+125°C^{+3°C}_{-0°C}$	Removes potential failures due to weak wire or chip bonding.
*External Visual	Method 2009	Removes defective units with respect to materials, construction, and workmanship.

* These tests are standard for both Models 1435 and 1435-83.

WARNING: To maximize frequency response the 1435 has NO input protection. Therefore, these precautions MUST be taken:

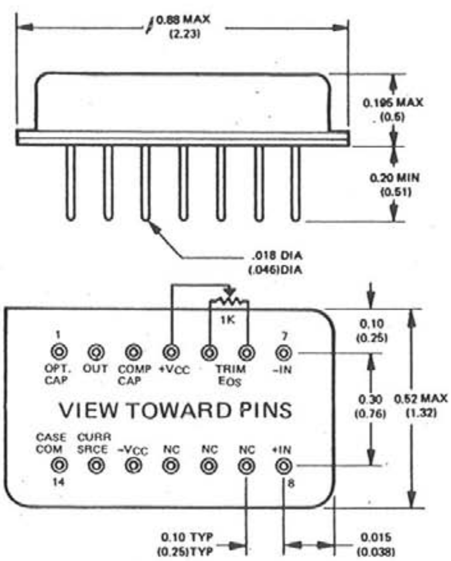
1. Do not apply $+V_{cc}$ before $-V_{cc}$
2. Do not apply Voltage to either input pin (7 & 8) prior to application of $\pm V_{cc}$

OR 3. Provide input protection per Figure 10.



Series diodes eliminate effects of diode capacitance on response.

Figure 10. Input Protection



Dimensions in parentheses are expressed in centimeters.
SCALE FACTOR: 1.7 : 1
Optional Socket: Augat Model 114-AG-2A

Figure 11. Mechanical Dimensions

To obtain the heat sinks mentioned here, please contact:
Thermalloy
2021 West Valley View Lane
Dallas, Texas 75234

TELEDYNE PHILBRICK

Allied Drive at Route 128, Dedham, Massachusetts 02026
Tel: (617)329-1600 TWX: (710)348-6726 Telex: 92-4439