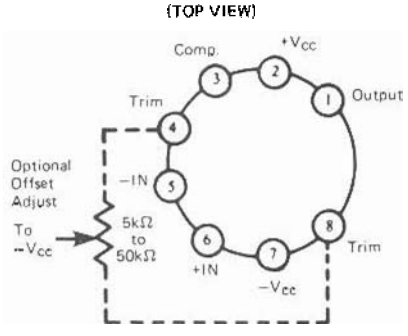
# Fast Settling, Fully Differential FET Input Op Amp

# 1443

The combination of high speed, wide bandwidth, excellent DC characteristics, and low-gain stability place the 1443 at the forefront of high performance operational amplifiers. Its 2GHz gain-bandwidth product, 1000V/$\mu$sec slew rate (when compensated for unity gain), and 130nsec settling time clearly make it an outstanding high speed device. Yet it has been carefully engineered to eliminate the low-gain stability problems that have historically plagued high frequency op amps. For example, as a unity gain follower, the 1443 has a small signal 3dB bandwidth of 120MHz, but still has 35° of phase margin with a 54pF capacitive load...using no exotic circuit techniques.

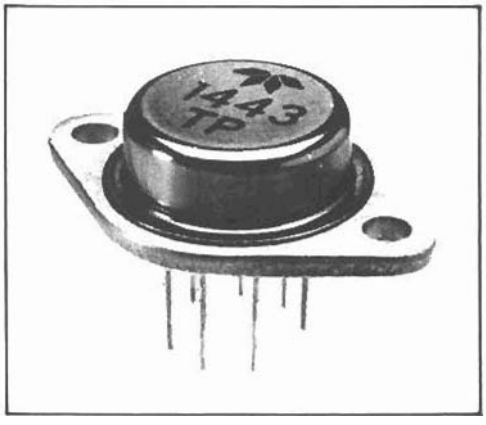
The 1443 has a fully differential FET input followed by a bipolar gain stage that together result in excellent DC characteristics. CMRR is 90dB minimum. Offset voltage and bias current are guaranteed less than ± 2mV and − 20pA respectively. Open loop gain is 100dB minimum. External compensation with a single capacitor allows users to tailor 1443 performance for different applications.

The 1443 is packaged in a TO-3 can, and the standard device is fully specified for 0°C to + 70°C operation. For military/aerospace applications, the 1443-83 is fully specified for − 55°C to + 125°C operation and screened to MIL-STD-883, Method 5008.




The metal case is electrically isolated. It is recommended that the case be grounded during use.

**Connection Diagram**




## FEATURES

- Excellent Low-Gain Stability
  80MHz Unity-Gain Bandwidth
  1000V/$\mu$s Slew Rate @ $A_{CL} = -1$
  ± 10V, ± 100mA Output
  130ns Settling to 0.01%
- 20pA Input Bias Current

## APPLICATIONS

- Video Instrumentation
- High Speed Follower
- Low Error Current Integrator Radar
- Video Frequency Filters
- Video Line Driver

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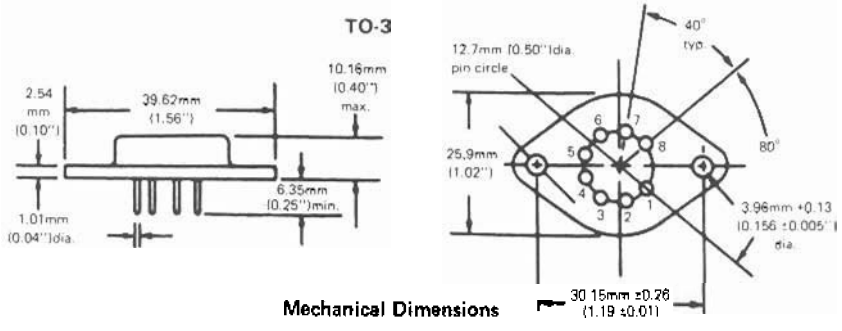
**SPECIFICATIONS** ( + 25°C, $V_{CC}$ = ± 15V, unless otherwise indicated)

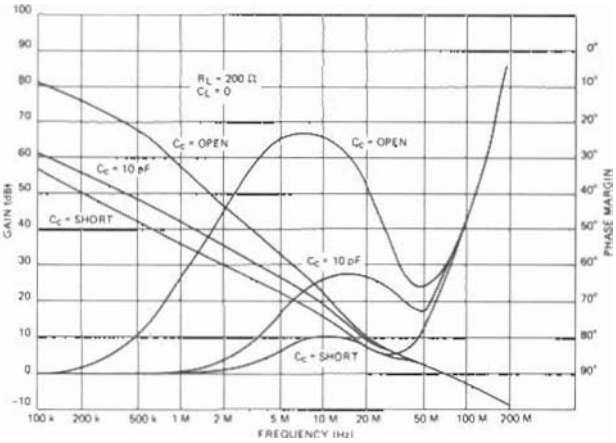
| | 1443 | | 1443-83 | |
|---|---|---|---|---|
| | **TYPICAL** | **GUARANTEED** | **TYPICAL** | **GUARANTEED** |
| **OUTPUT RANGE** | | | | |
| Voltage | ± 13 V | ± 10.25 V | ± 13 V | ± 10.25 V |
| Current | ± 130 mA | ± 100 mA | ± 130 mA | ± 100 mA |
| Short Circuit Current (Note 1) | ± 160 mA | | ± 160 mA | |
| **VOLTAGE GAIN (DC Open Loop)** | | | | |
| $R_L$ = 100Ω | 105 dB | 95 dB | 110 dB | 100 dB |
| **FREQUENCY RESPONSE** | | | | |
| Gain-Bandwidth Product (small signal) | | | | |
| f = 100kHz, $R_L$ = 200Ω, $C_C$ = open | 2.0 GHz | | 2.0 GHz | |
| f = 1MHz, $R_L$ = 200Ω, $C_C$ = 10 pF | 120 MHz | 90MHz | 130 MHz | 100 MHz |
| Unity-Gain Bandwidth | | | | |
| $R_L$ = 1kΩ, $C_C$ = short | 80 MHz | | 80 MHz | |
| Settling Time $R_L$ = 100Ω, $C_C$ = short | | | | |
| 10V Step to 1% | 50 ns | | 50 ns | |
| 10V Step to 0.1% | 80 ns | | 80 ns | |
| 10V Step to 0.01% | 130 ns | 165 ns | 130 ns | 150 ns |
| Slew Rate (Note 2) $R_L$ = 100Ω, $C_C$ = short | 1000 V/μs | 900 V/μs | 1200 V/μs | 1000 V/μs |
| Destabilizing Load Capacity | | | | |
| $R_L$ = 100Ω, $C_C$ = short, $A_{CL}$ = − 1 | > 300 pF | | > 300 pF | |
| **INPUT VOLTAGE RANGE/CMRR** | | | | |
| Common Mode for DC Linear Operation | ± 9 V | ± 7 V | ± 9 V | ± 7 V |
| Common Mode Fault, Absolute Max. | | ± $V_{CC}$ | | ± $V_{CC}$ |
| Differential Between Inputs | | 25 V | | 25 V |
| Common Mode Rejection Ratio | | | | |
| at DC | 90 dB | 80 dB | 100 dB | 90 dB |
| at 10MHz | 35 dB | | 35 dB | |
| **INPUT OFFSET VOLTAGE** | | | | |
| Initial (without external trim) (Note 3) | ± 1 mV | ± 3 mV | ± 0.5 mV | ± 2 mV |
| vs. Temperature | ± 50 μV/°C | ± 75 μV/°C | ± 25 μ V/°C | ± 50 μV/°C |
| vs. Power Supply (PSRR) | 90 dB | 80 dB | 90 dB | 85 dB |
| **INPUT BIAS CURRENT** | | | | |
| Initial | − 10 pA | − 50 pA | − 10 pA | − 20 pA |
| vs. Temperature | doubles every 10°C | | doubles every 10°C | |
| **NOISE** | | | | |
| DC to 10Hz | 50 μV (p-p) | | 50 μV (p-p) | |
| Above 10Hz | 20 nV/√Hz | | 20 nV/√Hz | |
| **POWER REQUIREMENTS** | | | | |
| Nominal Supply Voltage | ± 15 V | | ± 15 V | |
| Supply Voltage Range | | ± 12 V to ± 18 V | | ± 12 V to ± 18 V |
| Quiescent Current | ± 45 mA | ± 55 mA | ± 45 mA | ± 55 mA |
| **TEMPERATURE RANGE** | | | | |
| Specified (Case) | | 0°C to + 70°C | | − 55°C to + 125°C |
| Storage | | − 65°C to + 125°C | | − 65°C to + 125°C |

**SPECIFICATION NOTES**

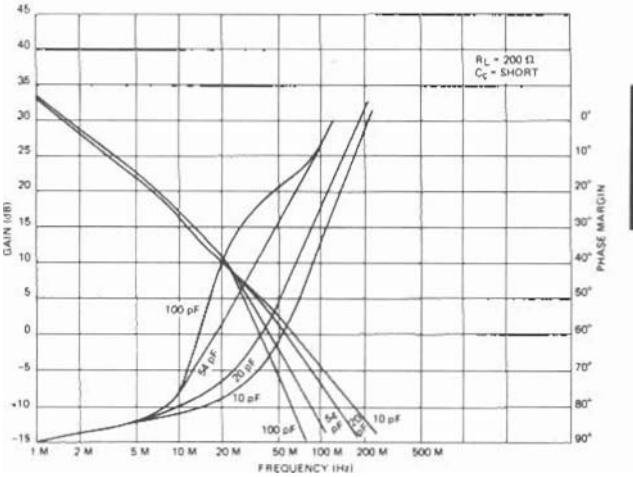
1. 1443 is not output short circuit protected. See Thermal Considerations.
2. $A_{CL}$ = − 1
3. Trimmable to zero. See Connection Diagram.



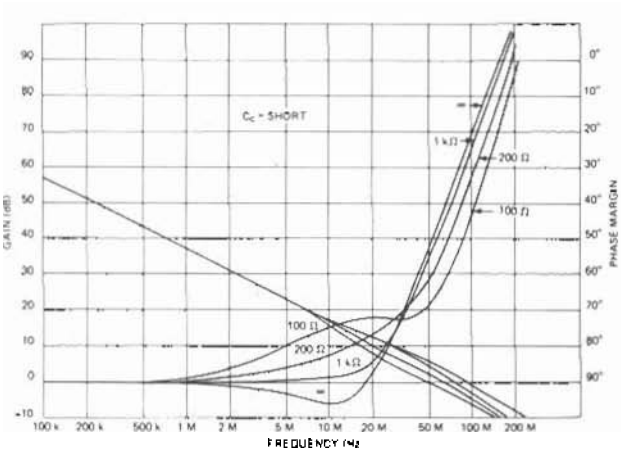

**Mechanical Dimensions**



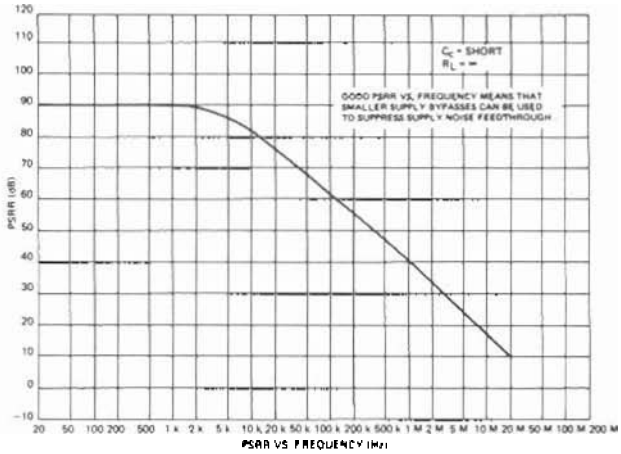

**Gain and Phase vs. Frequency for Variable Compensation**



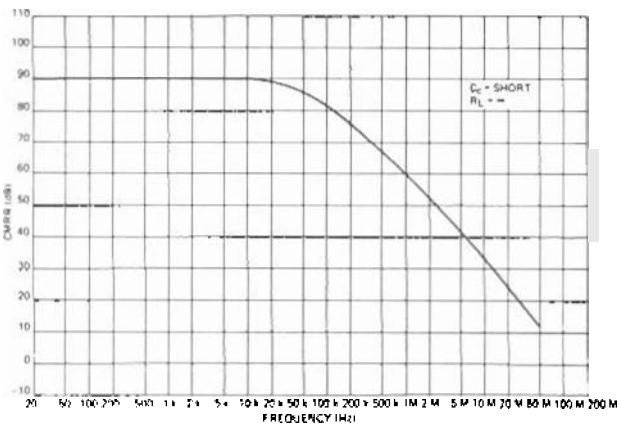

**Gain and Phase vs. Frequency for Variable $C_L$**



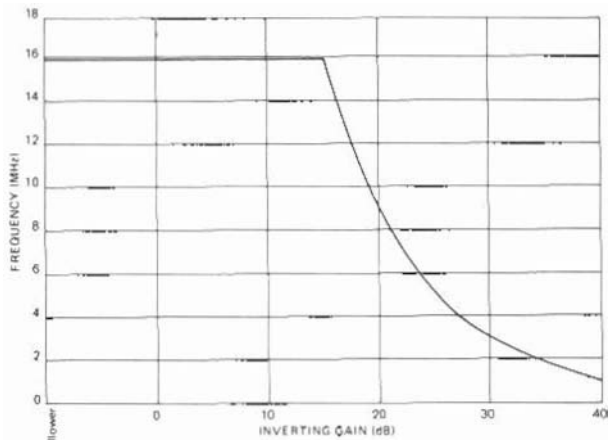

**Gain and Phase vs. Frequency for Variable $R_L$**




**PSRR vs. Frequency**




**CMRR vs. Frequency**




**Utilizable Full Power Bandwidth**

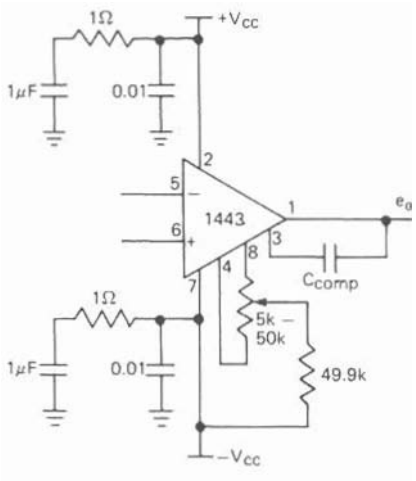
# Applications Information

## Compensation

The design of the 1443 allows users to "tailor" compensation/performance for different applications. The total effective compensation capacitance is an internal 5pF capacitor in series with whatever capacitor is placed between the compensation point (pin 3) and the output (pin 1).

To minimize low frequency (<1MHz) slewing error and to maximize bandwidth for higher gains (>30dB), the external compensation capacitor should range from open to 5pF. For best transient response at lower gains, use values greater than 5pF up to approximately 15pF. A short is recommended in lieu of a larger capacitor. Though the exact value of compensation will depend upon how much ringing and overshoot an application allows, most low-gain applications will find the best overall results by shorting pin 1 to pin 3.

Following the selection of a compensation capacitor ($C_{Comp}$), a feedback capacitor ($C_{FB}$) must be selected to properly compensate for input capacitance ($C_{FB} = 2pF/(NG-1)$. NG = noise gain which Teledyne Philbrick defines as $1/\beta$ where $\beta$ is equal to the fraction of the output signal that is fed back to the inverting input. Note that noise gain is the multiple of the amplifier input noise which will appear at the amplifier output. $C_{FB}$ may be increased to provide extra phase lead in case of low $C_{Comp}$. The choice of $C_{FB}$ is best made on the basis of permissible overshoot after $C_{Comp}$ has been chosen on the basis of gain.




1μF or larger tantalum supply bypass caps are recommended for fast settling applications.

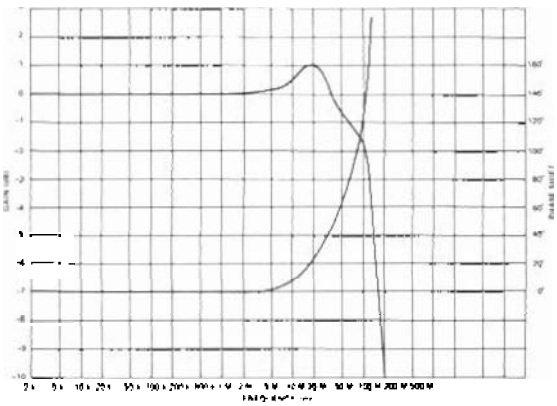
Typical Connection

## Bypassing

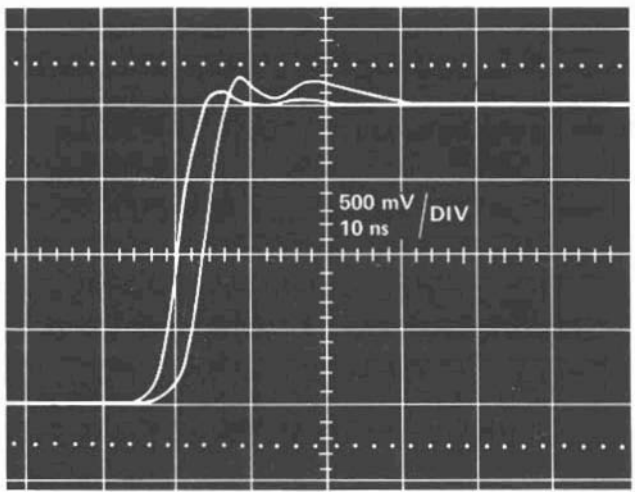
The traditional practice of decoupling power supply lines with bypass capacitors is necessary to prevent high frequency oscillations resulting from supply lead inductance and parasitic capacitance. Unfortunately, the bypass capacitor and lead inductance form a tank circuit that can ring when a step change in the op amp output forces a current pulse from the supply. In many cases, adding a dissipative element (a resistor) will damp the ringing. Its exact value is not critical, but the presence of the resistor is.

## Follower

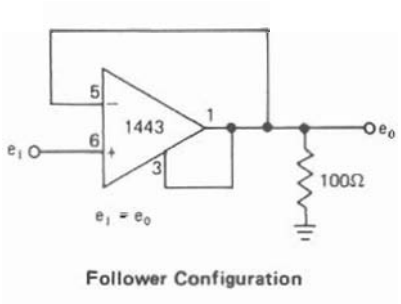
Impressive results can be obtained by using the 1443 as a unity gain follower—with a 3dB bandwidth of 120 MHz and only 1dB of peaking.



Frequency Response (As A Follower)



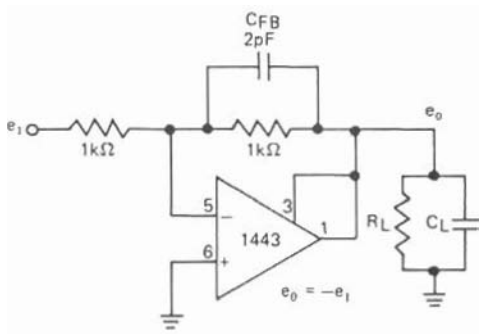

Follower Pulse Response




Follower Configuration

### Unity Gain Inverter

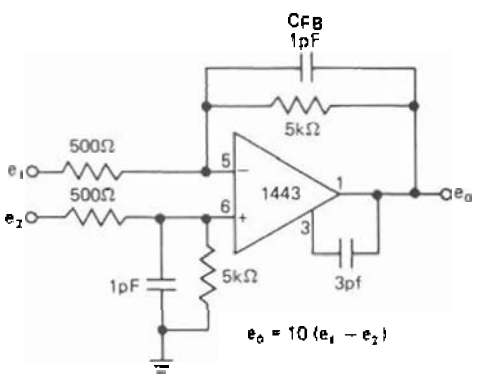
In this configuration, the 1443 has a typical 3dB bandwidth of 60MHz. It will settle quickly even if $C_L$ = 100pF and $R_L$ = 100Ω but will not oscillate if $R_L$ is open.




Unity Gain Inverter

### Differential Amplifier

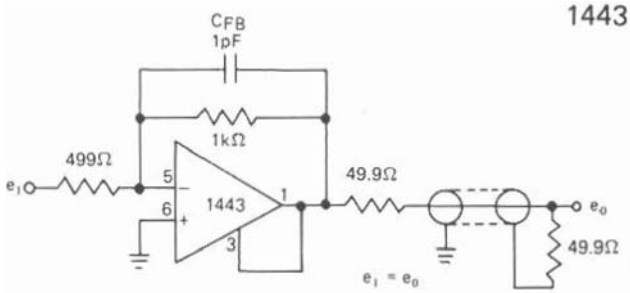
With its fully differential capabilities, the 1443 lends itself to many system configurations. Shown below is a typical configuration for a wideband (≅ 15MHz) differential amplifier.




Wide Band Differential Amplifier

### High Speed Co-Ax Driver

Use the 1443 as a cable driver with 50Ω terminating resistors at both ends (to minimize reflections) and drive a 50Ω cable to ±5V. Using 1% resistors and a 50Ω line, ghosts are down at least 77dB. With no resistor at the amplifier output, ghosts may only be down 38dB.




High Speed Co-Ax Driver

## High Frequency Troubleshooting Techniques

### Parasitic Oscillations

With VHF operational amplifiers like the 1443, it is not enough to be concerned only with stability problems due to loop closure (discussed in compensation section). Of equal concern and oftentimes more annoyance are parasitic oscillations. Parasitic oscillations are apt to arise in VHF op-amp circuits in which lead lengths are long (> ½ inch), or loop areas are large (> 1 sq. cm.) at the summing junction, feedback capacitor, power supply pins, or ground-return paths (from bypass capacitors or the amplifier case).

For the 1443, these oscillations may appear with frequencies up to 0.5GHz, and you cannot always count on seeing them with your oscilloscope. When such a parasitic oscillation occurs, it often appears as a DC offset because circuit conductance non-linearities detect its RF envelope. If what appears to be a DC offset is noisy and erratic, or responsive to the placement of your finger or a test probe, parasitic oscillations may be the problem.

Parasitic oscillations are also likely if there is any significant lead length separating the amplifier output from its load capacitance. The lead inductance and load capacitance form a series LC circuit that looks like a larger and larger capacitor as it approaches resonant frequency from below.

Even the lead lengths associated with attaching an oscilloscope probe can cause problems. For the typical Tektronix probe with the ground attached 10 cm. from the measurement point, the ground lead and probe form a series LC circuit of approximately 100nH and 12pF. At 100MHz (bandedge for the 1443), this will result in the apparent probe capacitance being double 12pF. In parallel with already existing circuit capacitances, this may be enough to cause oscillation. A good practice is to wrap the ground lead around the probe tip. An even better practice is to use a probe socket (Tek 131-0258-00) installed in the circuit with attention to the ground return route.

Semiconductor capacitances and bandwidths are highly nonlinearly dependent on voltages and currents. Devices that oscillate at one voltage level may not at another. As a minimum, check for op amp oscillations at zero output and at additional output points in each polarity. You will often find that oscillations exist at one or two points in the circuits' output range, and these may be observed only as unexplained perturbations on the output (they may not appear as bursts) due to envelope detection as previously discussed.

### The Finger as an Analog Development Tool

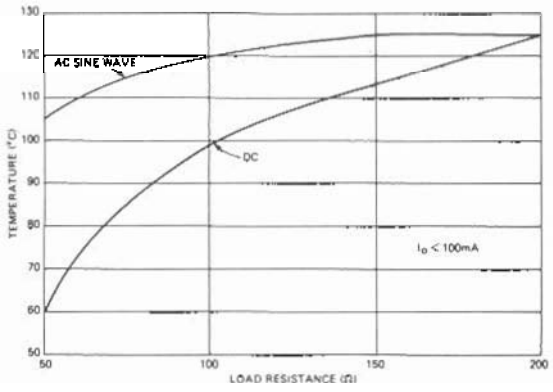
In 15 volt systems, the finger can be a useful investigative tool, if thoughtfully applied. It can couple signals in and out and also be used as a load. A well laid-out RF op-amp circuit will be only slightly affected by a light touch—dramatic differences reveal a sensitive point! Check by touching the amplifier case, the supply rails (carefully), ground, control knobs, chassis parts, etc. If things change markedly when you touch these areas, parasitics may well be the problem.

### Other Considerations

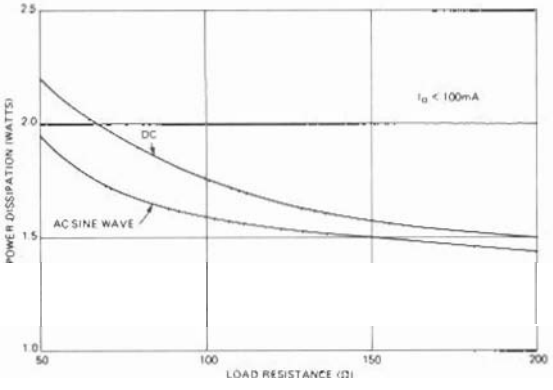
The problems commonly associated with video amplifiers are naturally present with VHF circuits. Therefore, the proper compensation of input capacitance by $C_{FB}$ cannot be ignored. Nor can the impedance (inductance) of ground return paths (though use of a ground-plane is helpful, it is no panacea).

### Thermal Considerations

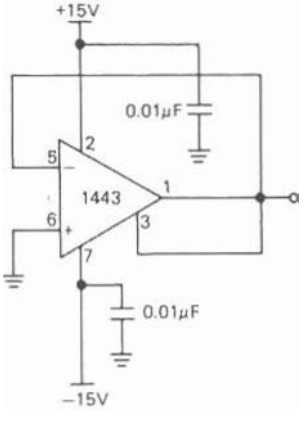
The 1443 has internal current limiting and can withstand an output short to ground if during the short the output current is negative as often as positive over each 100msec period. It is not short-circuit proof under all conditions. Maximum continuous junction temperatures should be kept below 150°C. $\theta_{CA} = 35$°C/Watt. $\theta_{JC}$ for the two output transistors is 95°C/Watt. With a 20Vp-p output sinusoid, the effective $\theta_{JC}$ of these transistors is 65°C/Watt. A heat sink is required above 75°C ambient (85°C for sinusoidal output) with a 200Ω load. With a 100Ω load, a heat sink is required above 40°C ambient (50°C for sinusoidal output).




**Maximum Allowable Case Temperature vs. Load Resistance With Worst Case Power Dissipation**




**Worst Case Power Dissipation vs. Load Resistance**




**Burn-In Test Circuit**



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