High Speed High Power VMOS Output Op Amp

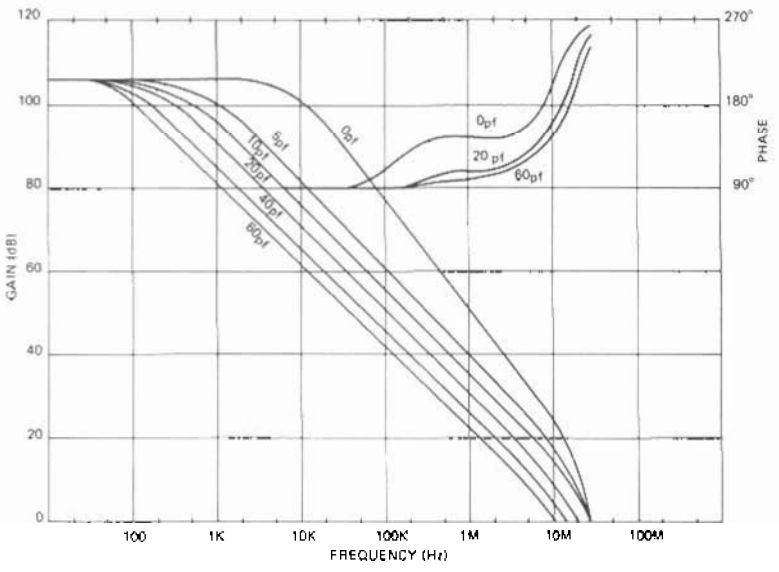
1461

The 1461 is an extremely fast, FET input, VMOS output, power op amp. It operates from ± 15V to ± 40V supplies and has output voltages up to ± 34V and output currents up to ± 750mA. Its unique VMOS output stage eliminates the safe operating area (SOA) restrictions and secondary breakdown problems that plague virtually all other presently available power op amps. The 1461's ability to handle high output currents at any voltage eliminates the normally intricate problems caused by driving capacitive or inductive loads.

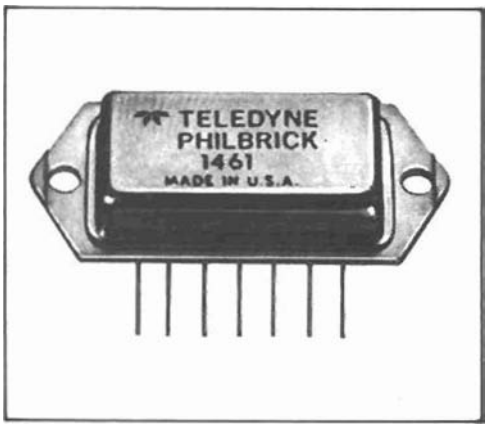
The 1461's combination of speed and power characteristics is unmatched. Even if it weren't a power amp, its 115dB open loop gain, 1GHz gain-bandwidth product, and 1200V/μsec slew rate would make it an outstanding high speed op amp.

The 1461 is packaged in a 14 pin dual-in-line with "ears" for easy mounting to heat sinks. Compensation is accomplished with a single external capacitor. Two external resistors are optional for current limiting.

The standard 1461 is specified for 0°C to + 70°C operation. For high reliability military/aerospace applications, it is available fully specified for − 55°C to + 125°C operation with MIL-STD-883 screening.



Bode Plot



FEATURES

- ± 30Volt, ± 600mA Output
- VMOS Output Stage
- No SOA Restrictions
- FET Input
- 1GHz GBW Product
- 1200V/μsec Slew Rate
  − 55°C to + 125°C Operation
  MIL-STD-883 Screening

APPLICATIONS

- Video Yoke Drivers
  Video Distribution Amplifiers
- High Speed ATE Pin Drivers
- High Accuracy Audio Amplification
- Driving Inductive and Capacitive Loads

TELEDYNE PHILBRICK Allied Drive @ Rte. 128, Dedham, Massachusetts 02026
Tel: (617) 329-1600, TWX: (710) 348-6726, Tlx: 92-4439

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($\pm V_{CC}$)	± 45 Volts
Differential Input Voltage	± 25 Volts
Common Mode Input Voltage	$\pm V_{CC}$
Output Short Circuit Current (Note 1)	± 800 mA
Operating Temperature Range (Case)	− 55°C to + 125°C
Specified Temperature Range (Case) (Note 2)	
1461	0°C to + 70°C
1461-83 (Note 3)	− 55°C to + 125°C
Storage Temperature Range	− 65°C to + 150°C

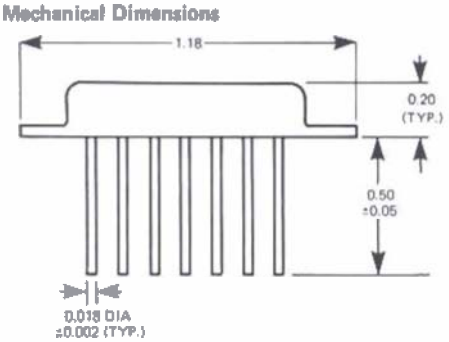
SPECIFICATIONS (+ 25°C, V_{CC} = ± 36V, unless otherwise indicated)

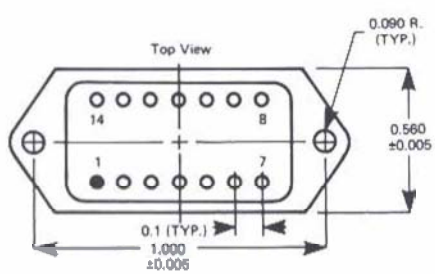
PARAMETER	MIN.	TYP.	MAX.	UNITS
OPEN LOOP VOLTAGE GAIN (R_L = 10kΩ)	100	115		dB
INPUT CHARACTERISTICS				
Offset Voltage: Initial		± 0.5	± 5	mV
Drift vs. Temperature		± 25	± 50	µV/°C
Drift vs. Supply (PSRR)		± 10		µV/V
Bias Current: Initial		± 10	± 100	pA
Drift vs. Temperature		Doubles every 10°C		
Common Mode Voltage for DC Linear Operation	± 25	± 28		Volts
Common Mode Rejection Ratio (Note 4)	90	100		dB
Noise (Referred to Input): 0.1Hz to 100Hz		4.5		µV(p-p)
100Hz to 10kHz		1.5		µV(RMS)
10kHz to 1MHz		6		µV(RMS)
OUTPUT CHARACTERISTICS				
Voltage Swing: R_L = 500Ω (Note 6)	± 27	± 29		Volts
R_L > 10kΩ	± 30	± 34		Volts
Current, ± 15V ≤ V_{CC} ≤ ± 40V	± 600	± 750		mA
FREQUENCY RESPONSE				
Gain-Bandwidth Product, C_C = 0pF, f = 100kHZ	800	1000		MHz
Unity-Gain Bandwidth, C_C = 20pF (Note 5)		15		MHz
Slew Rate: C_C = 0pF, R_L > 1kΩ	900	1200		V/µsec
C_C = 30pF, R_L > 1kΩ		150		V/µsec
Settling Time, C_C = 30pF, R_L = 500Ω				
25V Step to 0.1% (25mV)		0.5	1	µsec
25V Step to 1% (250mV)		350		nsec
10V Step to 0.1% (10mV)		400		nsec
10V Step to 1% (100mV)		250		nsec
POWER REQUIREMENTS				
Supply Voltage Range	± 15	± 36	± 40	Volts
Quiescent Current (Note 7)		± 20	± 25	mA

SPECIFICATION NOTES

1. Internally short circuit current limited. See Current Limiting section.
2. See Thermal Considerations section.
3. Processed to MIL-STD-883.
4. See Typical Performance Curve section for CMRR vs. frequency graph.
5. Teledyne Philbrick suggests the use of a 20pF compensation capacitor when using the 1461 in an inverting unity gain configuration. The recommended compensation for a follower configuration is 40pF.
6. See graph of maximum output voltage vs. output current.
7. See graph of quiescent current (R_L = open) vs. operating frequency.

Mechanical Dimensions





1 − In	8 Output
2 + In	9 + Current Limit
3 N.C.	10 + V_{CC}
4 N.C.	11 Compensation
5 − V_{CC}	12 Compensation
6 − Current Limit	13 Offset Adjust
7 N.C.	14 Offset Adjust

Applications Information

Compensation

The 1461 is externally compensated with a single capacitor. The gain bandwidth and slew rate of this device are related to the value of the capacitor by the following approximations:

$$\text{Slew Rate} \cong \frac{0.006}{C_{comp}} \text{ V/sec}$$

$$\text{Gain Bandwidth} \cong \frac{0.001}{C_{comp}} \text{ Hz}$$

These formulas are accurate for C_{comp} ranging down to a value of 5-10pF. At this point, circuit parasitics begin to take effect and limit the gain-bandwidth product to about 1GHz and the slew rate to approximately 1200V/μs.

In order to ensure stability when using the 1461, the value of the compensation capacitor must be such that the result of the gain-bandwidth product divided by the noise gain is less than 15MHz. This amplifier can maintain a 15MHz bandwidth up to noise gains of 40-50 by proper adjustment of the compensating capacitor.

Teledyne Philbrick defines noise gain = $1/\beta$ where β is equal to the fraction of the output signal that is fed back to the inverting input. Note that noise gain is the multiple of the amplifier input noise which will appear at the amplifier output.

Current Limiting

Internal to the 1461 are the two minimum-value resistors that limit the maximum output current to approximately 750mA. Output current can be further limited by the use of two external user-supplied resistors. One resistor ($+R_{sc}$) limits the positive current, and the other resistor ($-R_{sc}$) limits the negative current. To determine the value of the limiting resistors, the following approximation can be used:

$$\pm R_{sc} \cong \left(\frac{0.6}{I_{limit}} - 0.8 \right) \Omega$$

It is recommended that during initial amplifier testing, 10Ω resistors be used for $+R_{sc}$ and $-R_{sc}$. This will minimize the possibility of damage to the amplifier during circuit verification.

Thermal Considerations

The physics of standard bipolar output devices lead to a problem known as thermal runaway. This phenomenon is due to the fact that as a transistor gets hot, it conducts more current for any given V_{be}. The more current it conducts, the hotter it gets, eventually destroying itself. This phenomenon also occurs in small regions of the base of a transistor. If heat is not given time to dissipate from these hot spots, the transistor will destruct at power levels far below that which the device could normally withstand. This is called secondary breakdown and is the reason for safe operating curves on most power op amp data sheets.

The 1461 has a VMOS FET output stage. Since field effect transistors do **not** exhibit thermal runaway, they do **not** suffer from secondary breakdown problems. Output voltages and currents are limited only by power dissipation and not by safe operating curves. However, heat sinking may be required to ensure that maximum allowable junction temperatures are not exceeded. Example: on the 1461's thermal derating curves, the slope of the infinite heat sink line is 11°C/Watt. This is the thermal resistance (θ_{JC}) from each VMOS junction to case. Assume that one VMOS output transistor dissipates 5 Watts and the other dissipates 4 Watts. Further assume that the maximum ambient temperature (T_A) is 70°C and the maximum allowable junction temperature (T_J) is 150°C. The necessary thermal resistance (θ_{CA}) of the heat sink can be determined as follows:

1. Assume the device has a complementary output stage and that the thermal rise (junction-case) of each VMOS output transistor does not affect the other. Calculate the maximum amount of power dissipated for each of the two output devices (5 Watts and 4 Watts for this example). Using the higher power dissipation number, determine the maximum allowable case temperature (T_C).

$$T_J - P\,(\theta_{JC}) = T_C$$

$$150°C - (5 \text{ Watts}) \left(\frac{11°C}{\text{Watt}} \right) = T_C$$

$$T_C = 95°C$$

2. Calculate maximum total power dissipation (P_T) for the 1461 (assume ±36V supply and 20mA quiescent current).

$$(72V)\,(20mA) + \frac{5 \text{ Watts}}{VMOS_1} + \frac{4 \text{ Watts}}{VMOS_2} = P_T$$

$$P_T = 10.44 \text{ Watts}$$

3. Calculate the thermal resistance (θ_{CA}) of the heat sink needed to dissipate this power.

$$\frac{T_C - T_A}{P_T} = \theta_{CA}$$

$$\frac{95°C - 70°C}{10.44 \text{ Watts}} = 2.4°C/\text{Watt} = \theta_{ca}$$

Lead Inductance

The high frequencies and high current levels involved with the 1461 necessitate a closer look at the phenomenon of lead inductance. A single 22-gauge wire has a lead inductance of 0.636 μH/ft. This inductance can become significant when large rates of dI/dt are demanded at the output. For example, if as much as 4 inches of wire are used to connect pin 9 to pin 10 (the + current limiting terminals), this wire would show an inductance of 212nH. At 10MHz, this inductance would show an effective impedance of 13.3Ω. This resistance would limit the output current to only 42.5mA. If the unit were driving a 50Ω load, the effective slew rate would be limited to

$$\frac{dI}{dt} = \frac{0.6}{L} = 2.82A/\mu s$$

yielding a maximum slew rate of 141V/μs—far less than this device is capable of.

Skin Effect

Skin effect, though not quite as important as lead inductance, can also cause problems in the design of high-frequency, high-power products. The current flowing in a conductor establishes a magnetic field around the conductor. This causes the distribution of current flow to vary as a function of frequency. At higher frequencies, current is forced to the surface of the conductor, effectively yielding a much smaller wire. The effective resistance of the wire increases with the frequency according to the following formula:

$$R_{ac} = K\,(\sqrt{f})\,R_{dc}$$

where f is frequency in MHz and K is a factor that varies with wire size and type.

Example: a one-foot 22-gauge wire will have the following effective resistance at 10MHz:

$$K = 6.86$$

$$R_{dc} = 0.016\Omega/ft.$$

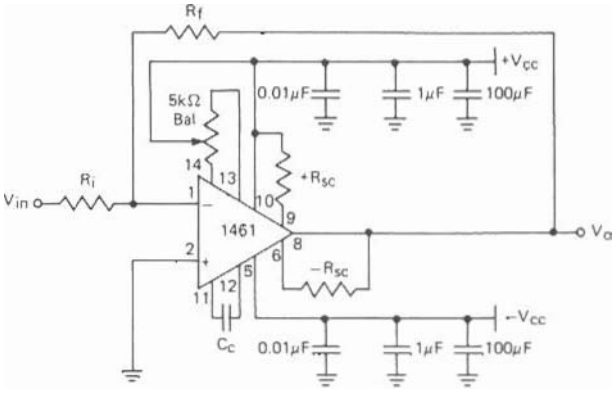
$$R_{ac} = (6.86)\,(\sqrt{10})\,(0.016) = 0.347\Omega$$

Even as little as 0.347Ω can decrease output current capabilities of the 1461 by as much as 30%.

It should be clear from this brief review of lead inductance and skin effect that short lead lengths are an absolute must in fast, high-power applications.

Standard Configuration

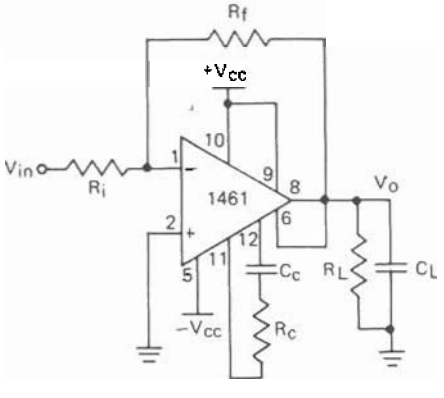
The 1461 in a standard inverting amplifier configuration including compensation capacitor, current limiting resistors, and offset adjusting potentiometer is shown below. To meet specified performance and avoid output oscillations, power supplies should be bypassed as shown. The 100μF capacitors are needed when driving heavy loads at high frequencies.



Standard Inverting Configuration

Capacitive Loads

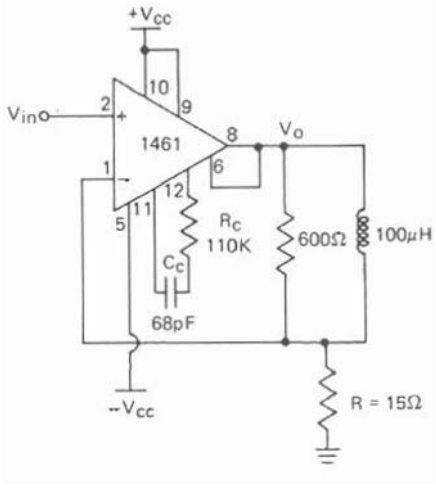
The 1461 can be used with a compensation network that can account for almost any value of capacitive load. First choose C_C for normal operation without a capacitive load. Then choose a series compensation resistor, R_C, such that $R_C C_C = R_{int} C_L$, where R_{int} is approximately 10Ω.



Capacitive Load Driver

Yoke Driver

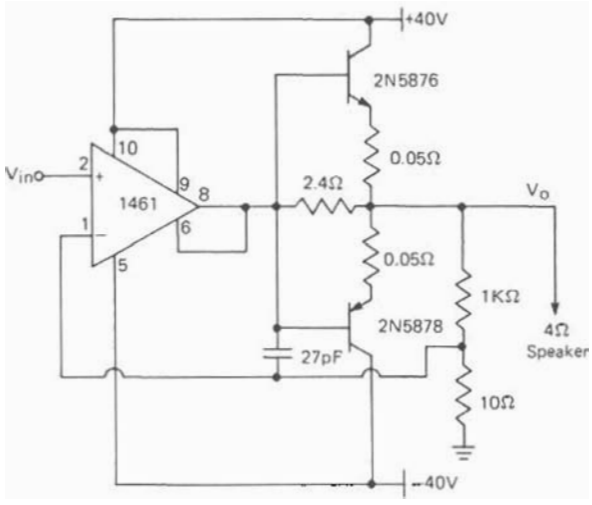
The absence of secondary breakdown makes the 1461 an excellent choice for driving electron beam deflection yokes, with settling times for a 0.5A step as low as 2-3μsec. For inductive load compensation, choose $R_C C_C = \frac{L}{R}$



Yoke Driver

Audio Amplifier

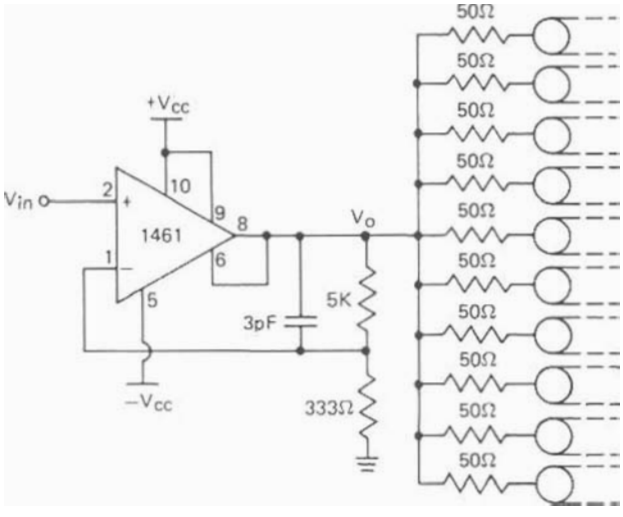
The 1461 has plenty of output current to drive the large base current requirements of high power transistors.



High Power Audio Amplifier

Video Amplifier

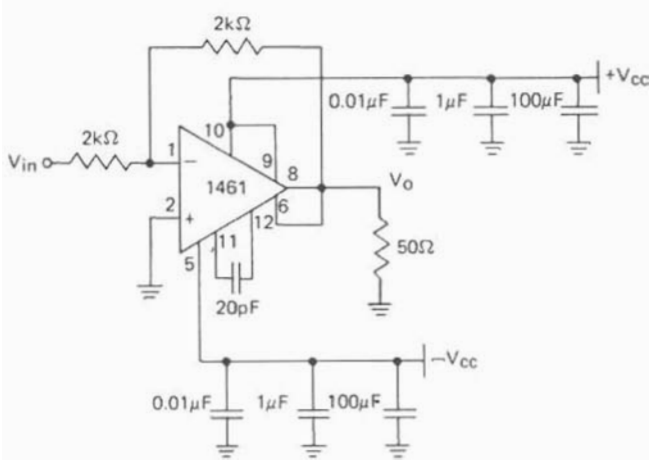
The 1461 as a video distribution amplifier can drive 10 coax cables directly. With a gain of 16, no compensation capacitor is needed.



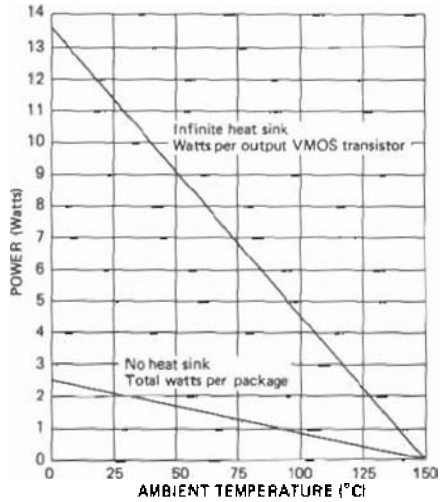
Video Distribution Amplifier

Inverting Unity Gain

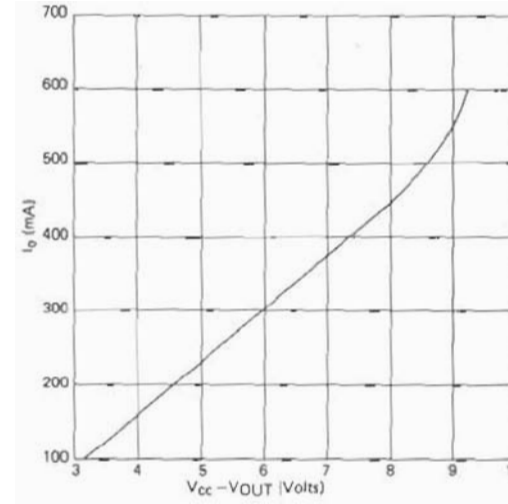
The 1461 can drive a 50Ω load in an inverting unity gain configuration. Recommended compensation is 20pF.



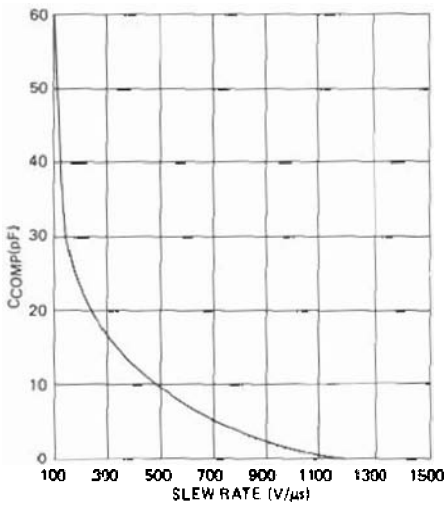
Inverting Unity Gain



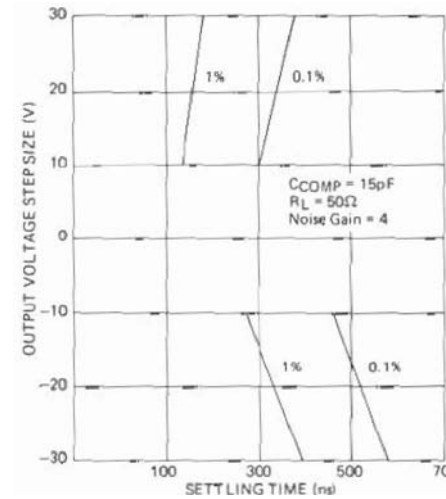
Power vs. Ambient Temperature



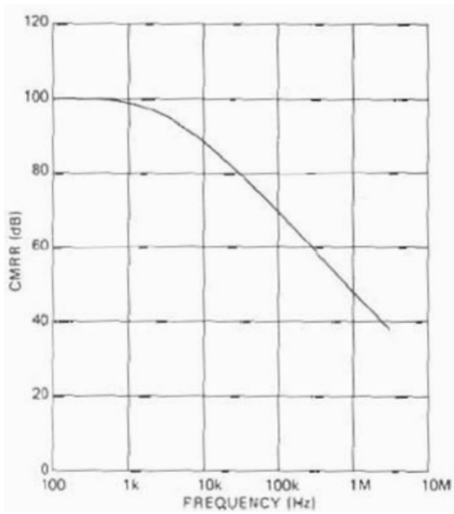
Guaranteed Output Voltage vs. Output Current



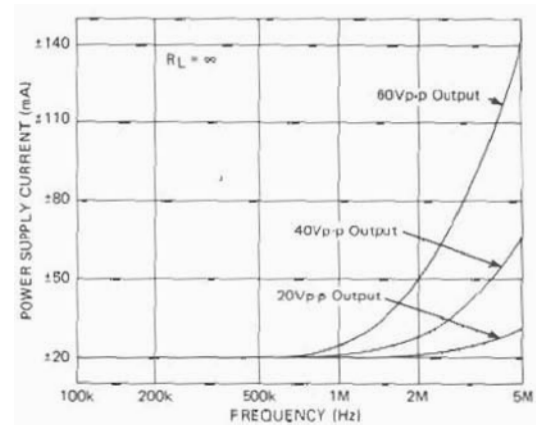
C_{comp} vs. Slew Rate



Output Voltage vs. Settling Time



CMRR vs. Frequency



Quiescent Current ($R_L = \infty$) vs. Operating Frequency

TELEDYNE PHILBRICK Allied Drive @ Rte. 128, Dedham, Massachusetts 02026
Tel: (617) 329-1600, TWX: (710) 348-6726, Tlx: 92-4439