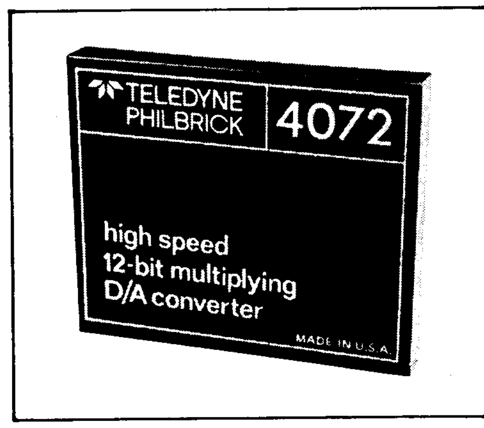
# 12 Bit, High Speed Voltage Output Multipyling DAC

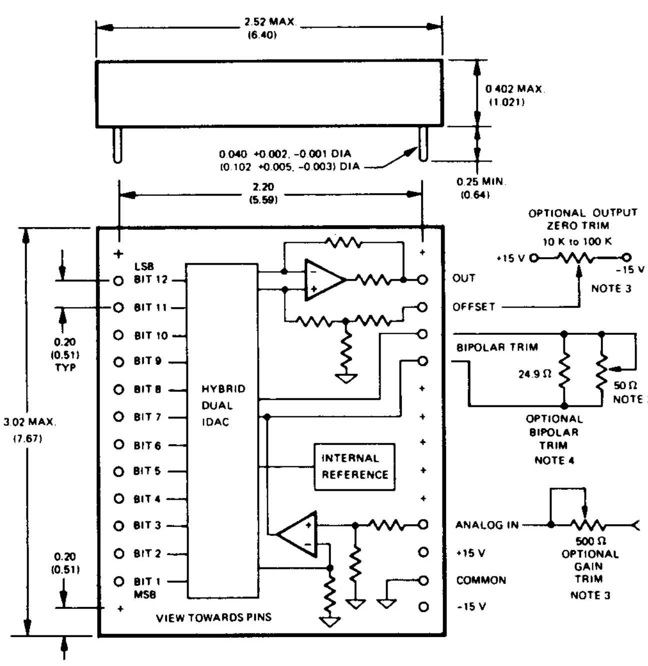
# 4072




The 4072 is a high speed, 12 bit, voltage-output multiplying D/A converter. It operates as a multiplier whose output voltage ( ± 10V) is the product of an analog input voltage, also called the reference voltage ( – 1V to + 10V), and a digitally programmable bipolar scale factor ( – 1 to + 1). The 4072 is TTL compatible and is a complete DAC including output amplifier. Gain and offset trim circuits are user optional.

The 4072 settling and bandwidth specifications are unmatched. With a fixed digital input, a step applied to the analog input results in an output step that settles to ± ½LSB in 750nsec maximum. With a fixed analog input, a change in digital input results in an output step that settles to ± ½LSB in 650nsec maximum. With a fixed digital code, the 4072 has analog input to analog output 3dB bandwidth of 7MHz. The full power bandwidth under these conditions is 1.5MHz.

The 4072 is a true 12 bit DAC. Integral linearity error is ± ½LSB maximum. Differential linearity error is guaranteed less than ± ½LSB. Around zero, differential linearity error is less than ± ¼LSB. The 4072 operates from ± 15V supplies, and power consumption is less than 1500mW.




## FEATURES

- Ultra Fast Settling
  750nsec Max Analog Step
  650nsec Max Digital Step
- 7MHz Bandwidth
- ± ½LSB Linearity
- Monotonicity Guaranteed Over Temperature
- Low Feedthrough

## APPLICATIONS

- High Fidelity CRT Displays
- Vector Generation
- Variable Gain Amplifier
- Waveform Synthesis

TELEDYNE PHILBRICK Allied Drive @ Rte. 128, Dedham, Massachusetts 02026
Tel: (617) 329-1600, TWX: (710) 348-6726, Tlx: 92-4439

**SPECIFICATIONS** (At +25°C, with ±15V supplies unless otherwise indicated.

| | Typical | Guaranteed |
|---|---|---|
| **INPUTS** | | |
| Analog | | |
| Voltage Range | --- | −1 to +10V |
| Resistance | 30KΩ | 31KΩ |
| Voltage Offset | --- | ±1mV |
| Voltage Offset vs. Temp. | 100μV/°C | --- |
| Max. Sine Frequency (10V P-P Input) | 1.5MHz | --- |
| Bandwidth −3 dB Small Signal (<1V P-P) | 7MHz | --- |
| Power | +14.7V to +15.3V @ 50mA max.<br>−14.7 V to −15.3V @ −50mA max. | |
| Recommended Philbrick Supply | 2212 | |
| Digital | | |
| Logic Code | Offset Binary | |
| Switching Levels | | |
| "0" State | --- | 0V to +0.8V @ <−40μA |
| "1" State | --- | +2.0V to +5.5V @ <+40μA |
| **TRANSFER CHARACTERISTICS** | | |
| Accuracy | | |
| Nonlinearity vs. Analog Input % of Input Span (10V) (See Note 2) | --- | ±0.02% |
| Nonlinearity vs. Digital Input % of Output Span (20V) (See Note 3) | --- | ±0.012% |
| Differential Nonlinearity vs. 10V Analog Input % of Output Span (20V) | --- | ±0.012% |
| Differential Nonlinearity vs. 2.5V Analog Input % of Output Span (20V) | --- | ±0.006% |
| Monotonicity and no missing levels | --- | +1 to +49°C |
| Output Noise DC −3MHz | 1mV · RMS | --- |
| Zero Offset Error % of Output Span (20V) | --- | Adjustable to 0 |
| Gain Error, Adjustable to 0 | --- | +0.3 to +1.3% |
| Analog · Digital Transfer | | |
| Scale Factor | | |
| (2Quadrant Digital, 1 + Quadrant Analog) | | |
| Digital Code 000...000 | --- | −1.000 |
| Digital Code 100...000 | --- | 0.000 |
| Digital Code 111...111 (20V Bipolar Span) | --- | +0.999512 |
| AC Analog Feedthrough | | |
| (0 to +10V Sine Wave at 100kHz | | |
| Digital Code 100...000 (See Note 1) | --- | ±1 LSB |
| DC Digital Feedthrough | | |
| (Bit Offset – All Digital Words) | | |
| 0V Analog In (See Note 1) | --- | ±¼ LSB worse case digital words |
| AC Analog Feedthrough | | |
| (0 to +10V Squarewave) | | |
| Digital Code 100...000 | Bipolar pulse typically −60mV, 40nsec followed by 24mV, 150nsec | |
| AC Digital Feedthrough (Glitch) | | |
| 0V Analog Input | | |
| All Bits Switching | Typically, 0.4V Peak, 60nsec wide triangular pulse, 24V nsec area | |
| Stability | | |
| Differential Nonlinearity vs. Temp. % of Output Span (20V) | --- | ±0.0005%/°C |
| Zero Offset Error vs. Temp. (for Output Span 20V) | --- | ±10ppm/°C |
| Gain Error vs. Temp. (for Output Span 20V) | --- | +30ppm/°C |
| PSRR % of Output Span (20V) | 0.002%/%$\Delta V_s$ | 0.006%/%$\Delta V_s$ |
| Dynamic Characteristics | | |
| Settling Time to ±½LSB (See Note 4) | | |
| Analog Input | | |
| 2.5V Output Step | 500nsec | --- |
| 10V Output Step | 650nsec | 750nsec |
| Digital Input | | |
| 10V Output Step | 400nsec | --- |
| 20V Output Step | 450nsec | 650nsec |
| Output Slew Rate | | |
| Analog Input Step | 50V/μsec | --- |
| Digital Input Step | 100V/μsec | --- |
| Rise Time, Small Signal, 0.1V Step | 40nsec | --- |
| Ramp Delay | | |
| Analog Input to Voltage Output | --- | 60 ±15nsec |
| Phase Shift, @ 20kHz | | |
| Analog Input to Voltage Output | −0.5 degrees | --- |
| **OUTPUTS** | | |
| Analog | | |
| Voltage Span | --- | 20V |
| Voltage Range | --- | −10V to +10V |
| Output Current | --- | ±40mA |
| Output Loading | | |
| Resistance | --- | 250Ω min. |
| Capacitance | --- | 100pF max. |
| **ENVIRONMENTAL SPECIFICATIONS** | | |
| Operating Temperature Range | --- | 0°C to +70°C |
| Storage Temperature Range | --- | −35 to +90°C |
| Relative Humidity | 100% non-condensing | --- |
| **ABSOLUTE MAXIMUM RATINGS** | | |
| Supply Voltages to Ground | --- | ±18V |
| Analog Input Voltage | --- | ±30V |
| Digital Input Voltage | --- | −0.5V to +5.5V |

NOTES:
1. The value of 1LSB is taken with +10V Analog Input
2. Input Span is defined as 10 Volts.
3. Output Span is defined as 20 Volts.
4. 4072 Settling Time to ±1LSB.

## Applications Information

The 4702's digital coding is offset binary. When the digital input is 000...000, the gain is −1. When the input is 111...111, the gain is +0.9951. When the input is 100...000, the output is zero. For applications requiring greater than specified accuracies, use the trimming procedures described below.

**Output Zeroing Trim Procedure** – Ground the Analog In pin and set the digital inputs to 100...000. Adjust the Output Zero Trim potentiometer for 0 Vdc output. (Should Output Zero Trim not be required, connect the offset pin to ground).

**Bipolar Trim Procedure** – Apply +10 Vdc to the Analog In pin and set the digital inputs to 100...000. Adjust the Bipolar Trim potentiometer for 0 Vdc output. (Should Bipolar Trim not be required, connect a 24.9 Ω resistor across the Bipolar Trim pins).

**Gain Trim Procedure** – Set the digital inputs to 000...000 and apply voltage to the Analog In pin. Adjust the Gain Trim potentiometer for an output with gain of −1. (Should Gain Trim not be required, connect a 249 Ω resistor in series with the Analog In pin).

**Power Considerations** – All models are provided with internal 1 μF power supply bypass capacitors. External power supply bypassing will only be required in exceptionally noisy environments.



**TELEDYNE PHILBRICK**
Allied Drive @ Rte. 128, Dedham, Massachusetts 02026
Tel: (617) 329-1600, TWX: (710) 348-6726, Tlx: 92-4439