# Monolithic CMOS 3½ Digit A/D Converter

# 4146

The 4146 is a 3½ digit monolithic CMOS analog-to-digital converter. It is fully self-contained in a 24 pin dual-in-line package and requires only a few passive support components for operation. Fully specified performance is guaranteed over the 4146's entire 0°C to +70°C operating temperature range.

A/D conversion is accomplished using an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of an unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero is counted. At the end of conversion, the total count is latched into the digital outputs as a 3½ digit binary word. Maximum integral and differential nonlinearities of ± ½LSB, typical power dissipation of 20mW, monotonic performance over the operating temperature range, and good temperature stability are only a few of the inherent characteristics of these monolithic devices.

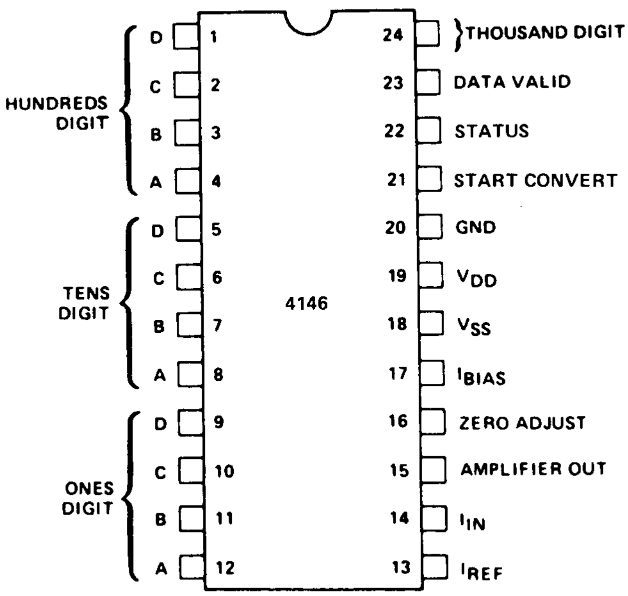
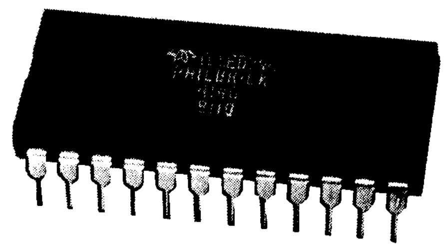



Figure 1. 4146 Pin Out



## FEATURES

- Low Power Dissipation
- Monolithic 24 Pin DIP Package
- No Missing Codes Over Temperature
- High Temperature Stability
- BCD Latched Output
- CMOS, TTL (Low-Power & LS) Compatible

## APPLICATIONS

- Data Acquisition
- Process Control
- Portable Measuring Equipment
- Low Cost Microprocessor Based Data Acquisition
- Tracking A/D Conversion

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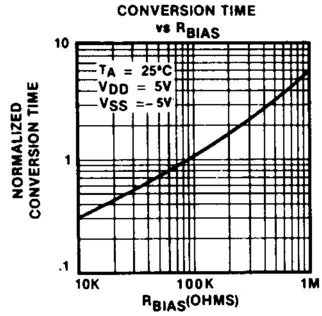
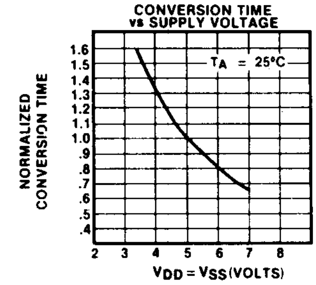
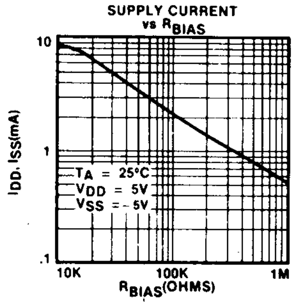
**SPECIFICATIONS** At 25°C with $V_{DD}$ = +5 V, $V_{SS}$ = −5 V, $V_{GND}$ = 0 V, $V_{REF}$ = −6.4 V, & $R_{BIAS}$ = 100 KΩ, unless otherwise specified.

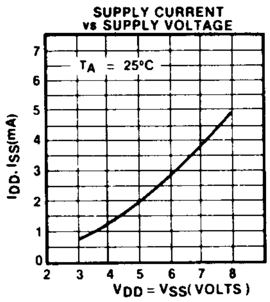
| | TYPICAL | GUARANTEED |
|---|---|---|
| **RESOLUTION** | | |
| 4146 | --- | 3½ digits |
| **Input** | | |
| Analog | | |
| $I_{IN}$ Full Scale ① | 10 μA | --- |
| $I_{REF}$ ① | −20 μA | --- |
| Power | | |
| $I_{DD}$ Quiescent | 1.4 mA | 2.5 mA |
| $I_{SS}$ Quiescent | −1.6 mA | −2.5 mA |
| $V_{DD}$ & $V_{SS}$ Operating Range | ±3 V to ±7 V | --- |
| Digital | | |
| Start Convert | | |
| Logic | CMOS or TTL (Low-Power & LS) | |
| Conversion Initiation | --- | "0" to "1" |
| Pulse Width, min. | --- | 500 nsec |
| Loading | --- | 1 CMOS Load |
| **TRANSFER CHARACTERISTICS** | | |
| Accuracy | | |
| Nonlinearity | --- | ±½ LSB |
| Differential Nonlinearity | ±¼ LSB | ±½ LSB |
| Zero Offset (Adj. to Zero) | ±10 mV | ±50 mV |
| Gain Error (Adj. to Zero) | ±2% | ±5% |
| Stability | | |
| (Diff.) Nonlinearity vs. Temp. | ±2.5 ppm/°C | ±5 ppm/°C |
| Zero Offset vs. Temp. | ±30 μV/°C | ±50 μV/°C |
| Gain Error vs. Temp. | ±25 ppm/°C | ±75 ppm/°C |
| PSRR, $V_{DD}$ & $V_{SS}$ = ±1 V | ±0.5%/V | ±1.0%/V |
| PSRR, $V_{DD}$ & $V_{SS}$ = ±1 V (Tracking) | ±0.05%/V | ±0.1%/V |
| Dyanmic | | |
| Conversion Time 4146 | 10 msec | 12 msec |
| **CONVERSION TIME IN FREE RUN MOSE** | | |
| 4146 | 10 msec | --- |
| **OUTPUTS** | | |
| Digital | | |
| Logic Codes | | |
| Parallel, Unipolar | BCD | |
| Output Drive | --- | 5 LP TTL Loads |
| Switching Levels, all digital outputs | | |
| "0" State | --- | ≤ .4 V |
| "1" State | --- | ≥2.4 V |
| Data Valid, "1" state for valid data | 5 μsec | --- |
| Status | | |
| "1" State | During Conversion | |
| Output Drive | --- | 5 LP TTL Loads |
| **ENVIRONMENTAL SPECIFICATIONS** | | |
| Operating Temp. Range 4146 | --- | 0°C to +70°C |
| Storage Temp. Range | --- | −65°C to +150°C |
| **ABSOLUTE MAXIMUM RATINGS** | | |
| $V_{DD}$ − $V_{SS}$ | --- | 18 V |
| $I_{IN}$ | --- | ±10 mA |
| $I_{REF}$ | --- | ±10 mA |
| Digital Input Voltage | --- | −0.3 V to $V_{DD}$ +0.3 V |
| Package Dissipation | --- | 500 mW |
| Lead Temperature (10 seconds) | --- | 300°C |

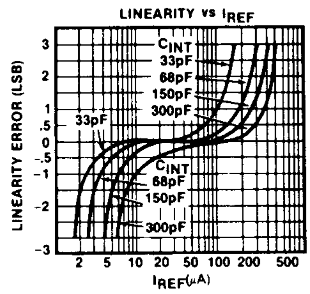
① This pin is connected to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Figure 2.




## HANDLING PRECAUTIONS

The **4146** series are CMOS devices and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

## APPLICATIONS

**Input/Output Relationships** – The analog input voltage ($V_{IN}$) is related to the output by the transfer equation:

$$\text{DIGITAL COUNTS} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

$$A = 4128$$

where DIGITAL COUNTS is the value of the BCD output word presented at Digits Out pins in response to $V_{IN}$.

The digital output code format is as follows:

| ANALOG INPUT | DIGITAL OUTPUT |
|---|---|
| $V_{IN} \geq$ Full Scale | 1100110011001 |
| = Full Scale – 1 LSB | 1100110011001 |
| = 1 LSB | 0 . . . 000 . . . 1 |
| $\leq 0$ | 0 . . . 000 . . . 0 |

**External Component Selection** – Obtaining a high accuracy conversion system depends on the voltage regulation of $V_{REF}$ and the thermal stability of $R_{IN}$ and $R_{REF}$. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of $V_{DD}$ and $V_{SS}$. The supply connections $V_{DD}$ and $V_{SS}$ should have bypass capacitors of value 0.1 $\mu$F, or larger, right at the device pins.

**$R_{IN}$, $R_{REF}$** – Values of these components are chosen to give a full scale input current of approximately 10 $\mu$A and a reference current of approximately –20 $\mu$A.

Examples:

$$R_{IN} \cong \frac{V_{IN}\ \text{FULL SCALE}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}$$

$$R_{IN} \cong \frac{10\ V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4\ V}{-20\ \mu A} = 320\ K\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of $R_{IN}$ typically would be trimmed using the optional gain adjust circuit to obtain full scale output at $V_{IN}$ FULL SCALE (see adjustment procedure.) Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

**$R_{BIAS}$** – Specifications for the 4146 are based on $R_{BIAS}$ = 100 K$\Omega$ ±10% unless otherwise noted.

Where only intermittent duty is required, additions can be made to the bias circuit to permit lower power usage during standby operation. (Example) The $R_{BIAS}$ resistor sets the current through the integrating amplifier and regulates the conversion rate. By switching in a larger value of resistance during the shutdown period the quiescient current can be reduced by an order of magnitude. During the shutdown period, data in the output latches is unaffected and continues to be available.

**$R_{DAMP}$** – Exact value not critical but should have a nominal value of 100 $\Omega$ ±10%. Locate close to pin 14.

**$C_{DAMP}$** – Exact value not critical but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

**$C_{INT}$** – Exact value not critical but should have a nominal value of 68 pF ±10 %. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15.

**$V_{REF}$** – A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

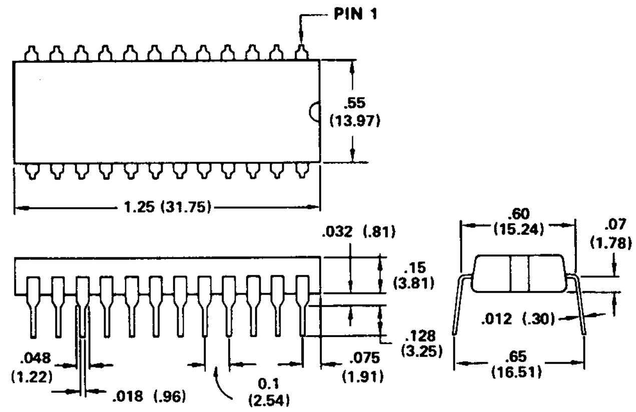
**$V_{DD}$, $V_{SS}$** – Power supplies of ±5 V are recommended, with 0.05% line and load regulation and 0.1 $\mu$F decoupling capaciters.

**Adjustment Procedure** – The test circuit diagram shows optional circuits for trimming the zero location and full scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full scale), it is recommended that transition points be used in setting the zero and full scale values. Recommended procedure is as follows:

1. Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
2. Set $V_{IN}$ to +½LSB and trim the zero adjust circuit to obtain a 000. . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
3. For full scale adjustment, set $V_{IN}$ to the full scale value less 1½ LSB and trim the gain adjust circuit for a 1100110011000 to 1100110011001 transition.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

## PHYSICAL DIMENSIONS




All dimensions are typical values unless stated otherwise. Dimensions in parentheses are expressed in millimeters.

4146 24-Pin Plastic DIP

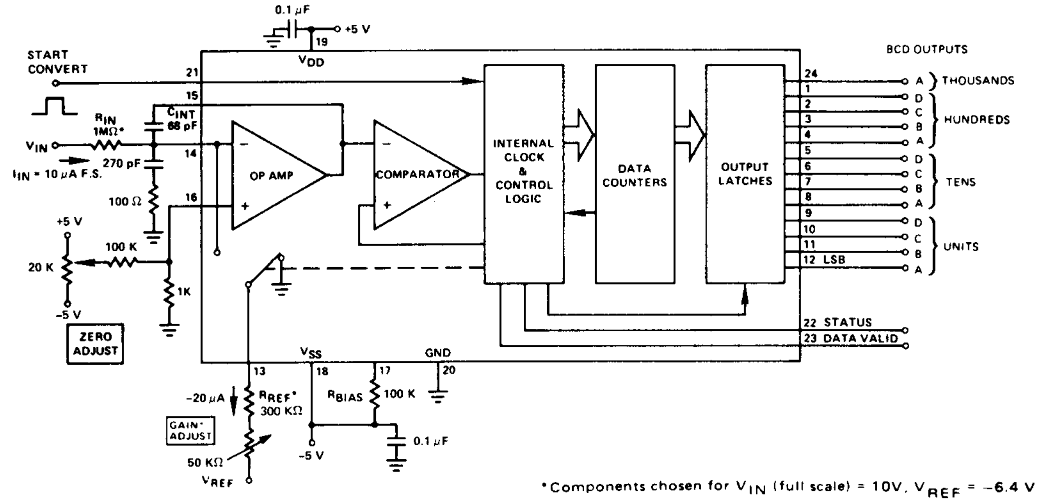



**Figure 2. Functional Block Diagram**

## CIRCUIT DESCRIPTION

During conversion the sum of a continuous current $I_{IN}$ and pulses of a reference current $I_{REF}$ is integrated for a fixed number of clock periods. $I_{IN}$ is proportional to the analog input voltage; $I_{REF}$ is proportional to the reference voltage and is of opposite sign to $I_{IN}$. $I_{REF}$ is switched in for exactly one clock period just frequently enough to maintain the summing input of the integrator near zero. Thus, the charge from the continuous $I_{IN}$ current is balanced against the pulses of $I_{REF}$ current. The total number of $I_{REF}$ pulses needed during the conversion period to maintain the charge balance is counted, and the result (in BCD) is latched into the outputs at the end of conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end of conversion routine. The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the $I_{REF}$ current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Start Convert input is strobed with a positive signal, the Status line is latched high and a 10 μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5 μs. This binary sequence is shown in the timing diagrams. Status is true high, and when the circuit is converting, Start Convert has no no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

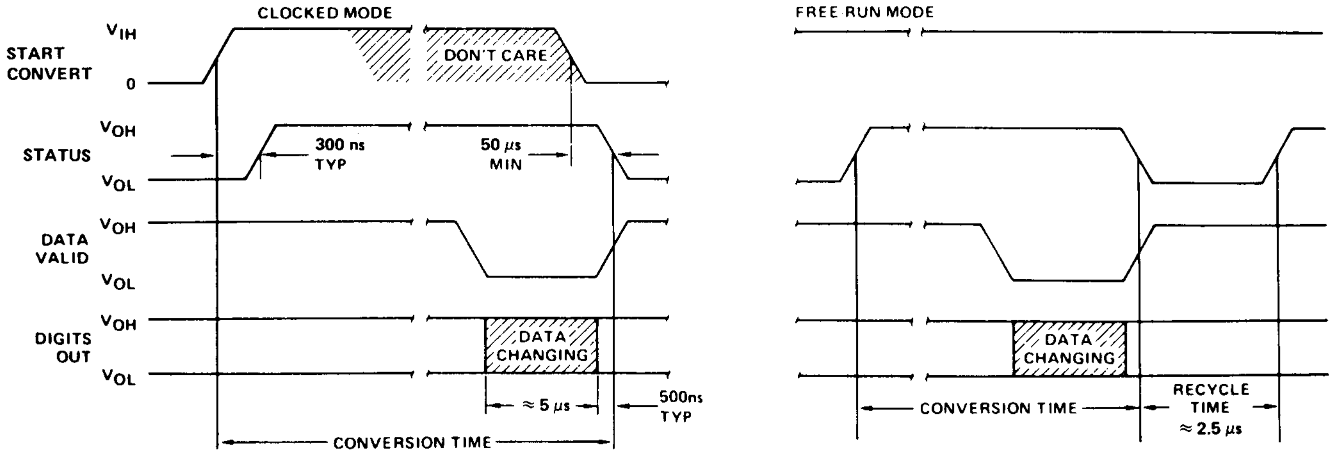



**Figure 3. Timing Diagrams (Rise, fall times = 200 ns typ., $C_L$ = 50 pF)**



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