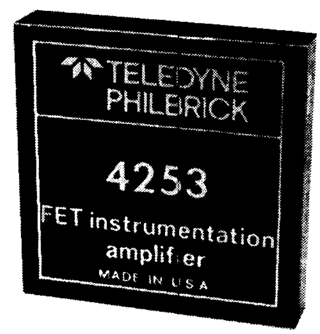
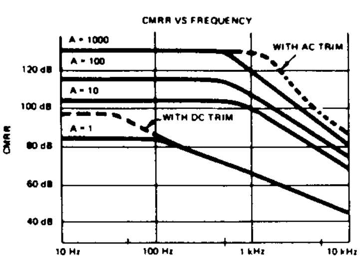
High Performance FET Input Instrumentation Amplifier

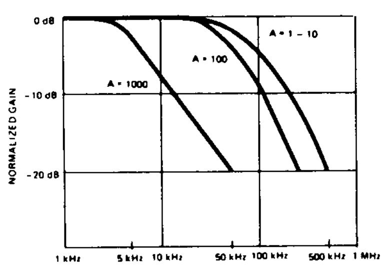
4253

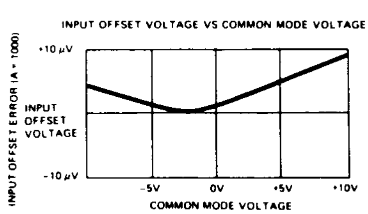
The 4253 is a high performance, FET input instrumentation amplifier designed to extract small differential signals from large common mode input voltages and accurately amplify them with gains to 10,000. A unique bootstrapped FET input circuit provides a very high, $10^{13}\Omega$, input impedance, minimizing source loading errors. Manufactured with precision active and passive components, the 4253 is computer tested ensuring high frequency stability, low nonlinearity error ($\pm 0.005\%$FS), excellent CMRR (including AC, DC signals and large unbalanced sources) and low temperature drifts. By applying an optional external reference, the user is able to adjust the output for both narrow and wide voltage ranges.

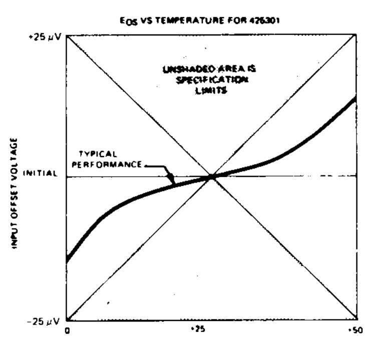
4253 is ideal for applications that require high input impedance, high CMRR, low input noise and low offset voltage drift. These include various types of transducers and signal conditioners. When applying this fixed-gain amplifier in data acquisition applications, signal-to-noise ratio is increased, common-mode noise pickup virtually eliminated, and system accuracy guaranteed.











FEATURES

- 75kHz Unity Gain Bandwidth
- $10^{13}\Omega$ Input Impedance
- -10pA Max Input Bias Current
- 114dB CMRR
- 0.7μVrms Input Noise
- Bipolar Input Offsetting

APPLICATIONS

- Low Level Instrumentation
- High Resolution Control Loops
- High Impedance Sensors
- Pressure Transducers
- Bridge Amplifiers
- Biomedical Engineering

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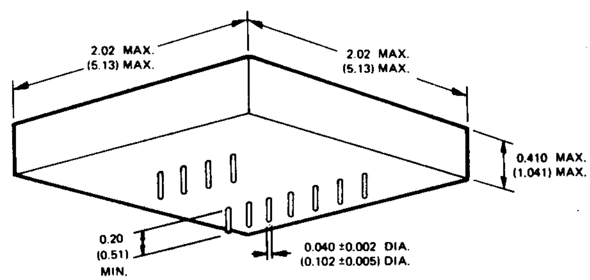
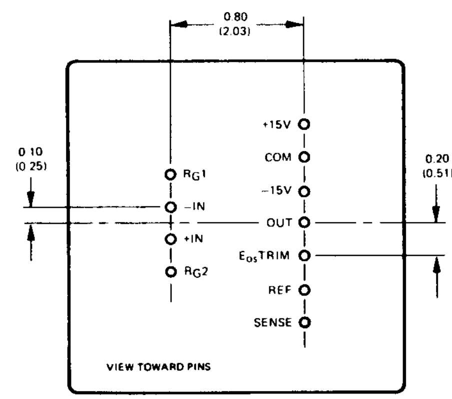
SPECIFICATIONS Typical @ 25°C and ±15V power unless otherwise specified

GAIN, A	
Gain Equation	$1 + \frac{100\,k\Omega}{R_G}$
Range of Gain	1 to 10,000
Gain Accuracy (R_G = 100Ω, 1%)	±2%
Gain	1.002 max (when Rg = ∞)
Gain Nonlinearity, max ①	
A = 1	0.05%
A = 10, A = 100	0.005%
A = 1,000	0.01%
Gain Non Linearity Temp Coefficient	
A = 1	1 ppm/°C
A = 10 to 1000	0.5 ppm/°C
Gain Temperature Coefficient, max (0°C to +50°C)	
A = 1	20 ppm/°C
A = 10, A = 100, A = 1000	30 ppm/°C
OUTPUT	
Rated Output, min	±10V @ ±5 mA
Output Impedance, A = 1, dc	< 0.1 Ω
Output Impedance, A = 1, f = 3 kHz	1.0 Ω
Cap Load Without Instability	0.01 μF
INPUT	
Input Impedance-Differential	10^{13}Ω ‖ 3 pF
Input Impedance-Common Mode	10^{13}Ω ‖ 3 pF
Input Voltage Range-Differential, Abs.Max	±36 V
E_{cm}, Common Mode Voltage Range Linear Operation, (Min) ②	±10 V or $\pm(12 - A\left\lvert\frac{E_{IN(PK)}}{2}\right\rvert)$V (smaller of above)
E_{cm}, Fault, Abs. Max	±18 V
Common Mode Rejection, CMR, min	
dc to 60 Hz, A = 1, A = 10	76 dB
dc to 100 Hz, A = 1000	114 dB
dc to 500 Hz, A = 1000 (with optional ac trim) ③	108 dB
OFFSETS AND NOISE	
Offset Voltage, E_{os}, Initial @ 25°C	
E_{os} RTI, max	±1.0 mV
E_{os} RTO, max	±15 mV
Offset Voltage Temperature Coefficient ④	
E_{os} TC, RTI (0 to +25°C, +25°C to +50°C), max	±10 μV/°C
E_{os}, TC, RTI (−25 to +85°C), typ.	±10 μV/°C
E_{os}, TC, RTO (0 to +50°C), max	±100 μV/°C
Voltage Noise, RTI	
0.016 to 1.6 Hz, Peak-to-Peak	2 μV
1.6 to 160 Hz, rms	0.3 μV
160 Hz to 16 kHz, rms	0.7 μV
Voltage Noise, RTO	
0.016 to 1.6 Hz, Peak-to-Peak	30 μV
1.6 to 160 Hz, rms	30 μV
160 Hz to 16 kHz, rms	60 μV
Offset Voltage vs Power Supply, RTI, max	±3 μV/%
Offset Voltage Time Drift, RTI (@ Constant Temp)	
Per day	±5 μV
Per Month	±12 μV
Per Year	±50 μV
DYNAMIC RESPONSE	
Small Signal Frequency Response for 1° Phase Shift (approximately 0.015% amplitude error)	
A = 1, A = 10	1 kHz
A = 100	500 Hz
A = 1000	100 Hz
Small Signal Frequency Response for ±3 dB Flatness	
A = 1, A = 10	75 kHz
A = 100	40 kHz
A = 1000	5 kHz
Small Signal Frequency Response for 1% Flatness.	
A = 1 to 10	5200 Hz
A = 100	2800 Hz
A = 1000	350 Hz
Large Signal Frequency Response Undistorted Full Output (f_s), All Gains, min	5 kHz
Settling Time to 0.1% (Step Input)	
A = 1, A = 10, A = 100	25 μsec
A = 1000	250 μsec

INPUT BIAS CURRENT, I_B	
Initial at +25°C, max	−10 pA
I_B Temperature Coefficient, 0 to +50°C	Doubles every +10°C
Slope at +25°C max	1 pA/°C
Input Bias Current at +50°C, max	−55 pA
I_B Vs E_{cm}	0.05 pA/V
I_B Vs E_{in}	0.05 pA/V
I_B Vs Power Supply	0.02 pA/%
Input Current Noise	
0.016 to 1.6 Hz, peak-to-peak	0.1 pA
1.6 Hz to 160 Hz, rms	1 pA
160 Hz to 1.6 kHz, rms	2 pA
POWER REQUIREMENTS	
Nominal Supply Voltage, $\pm V_{CC}$	±15 V
Voltage Range	±12 V to ±18 V
Current: Quiescent	±16 mA
Current: Full Load	±21 mA
TEMPERATURE RANGE	
Operating: Rated	0 to +50°C
Operating: Derated	−40 to +85°C
Storage	−55 to +125°C

NOTES
* Indicates same specification as 4253
① Peak-to-Peak deviation from best straight line
② Refer to application note on common mode voltage range for detailed explanation
③ Refer to procedure for optional CMR trim
④ Measured without external trim





±0.01 Non-cumulative tolerance between pins
±0.02 Tolerance from case edge to center of pin

DIMENSIONS IN PARENTHESES ARE EXPRESSED IN CENTIMETERS

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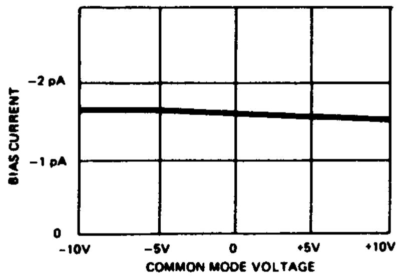
BIAS CURRENT VS COMMON MODE VOLTAGE



APPLICATION NOTES

GAIN

The gain of the 4253 is adjustable from 1 to 10000 by one external resistor according to the formula:

$$A = 1 + \frac{100k}{R_G}$$

R_G should be a high-quality, low temperature coefficeint resistor for maximum gain stability.

OFFSETS & NOISE

General

Connect "Ref" to "Common" if output offset trim is not used.

Offset voltage errors and noise voltages appearing at the output of the 4253 are dependent upon RTI and RTO values, as well as the amplifier gain (A), and can be calculated by the following equation:

$$E_o = A \cdot E_{RTI} + E_{RTO}$$

Offsets RTI (High Gain)

If a slight degradation in $E_{OS}TC$ (RTI) can be tolerated, the "E_{OS} Trim" terminal can be used to correct the initial input offset voltage of the 4253 plus a few millivolts of signal offset. To zero the initial E_{OS}, set A = 100 or 1000, connect the "+In", "–In", and "Ref" inputs direct to " Com" (common), and trim for minimum output voltage. The recommended trim network is shown in the Functional Block Diagram (See Figure 1).

If not used, the "Input E_{OS} Trim" terminal should be left floating. Unlike many competitive amplifiers, the $E_{OS}TC$, RTI, of the 4253 is not significantly affected by the common mode voltage.

Output Offsetting Capability

The output of the 4253 may be biased or offset up to ±10 volts from ground by applying a reference voltage to the "Ref" pin. This permits the user to offset such things as tare weight in a load-cell application, barometric pressure in an absolute pressure measuring system, etc. In cases where the gain is constant, this also permits compensation for input offsets without affecting the $E_{OS}TC$ (RTI).

The input impedance to the "Ref" terminal is approximately 10MΩ. The output offset will equal the applied reference voltage. Two recommended trim circuits, one for wide range and one for narrow range, are shown in Figure 1.

If the output offset capability is not required, the "Ref" pin must be connected directly to the "Com" pin.

COMMON MODE VOLTAGE RANGE

The input common mode voltage (E_{cm}) is defined as the average of the voltages at the two input terminals. With no differential input signal (E_{in} = 0), the linear E_{cm} range of the 4253 is ±10 volts minimum. It decreases slightly as a function of E_{in} (Peak) and the gain (A), as indicated in the equation shown below.

$$E_{cm}\ \text{Range} = \pm\left(12 - A\left|\frac{E_{IN(PK)}}{2}\right|\right)V = \pm\left(12 - \left|\frac{E_{O(PK)}}{2}\right|\right)V \text{ or } \pm 10\ V$$

SMALLER OF ABOVE

$$\text{Where } E_{cm} = \frac{E_{-In} + E_{+In}}{2}$$

COMMON MODE REJECTION

The excellent common mode rejection of the 4253 is specified at the full ±10 volt E_{cm} range. For critical applications, the CMR can be trimmed for peak performance for both ac and dc by following the optional trim procedure shown in Figure 2.

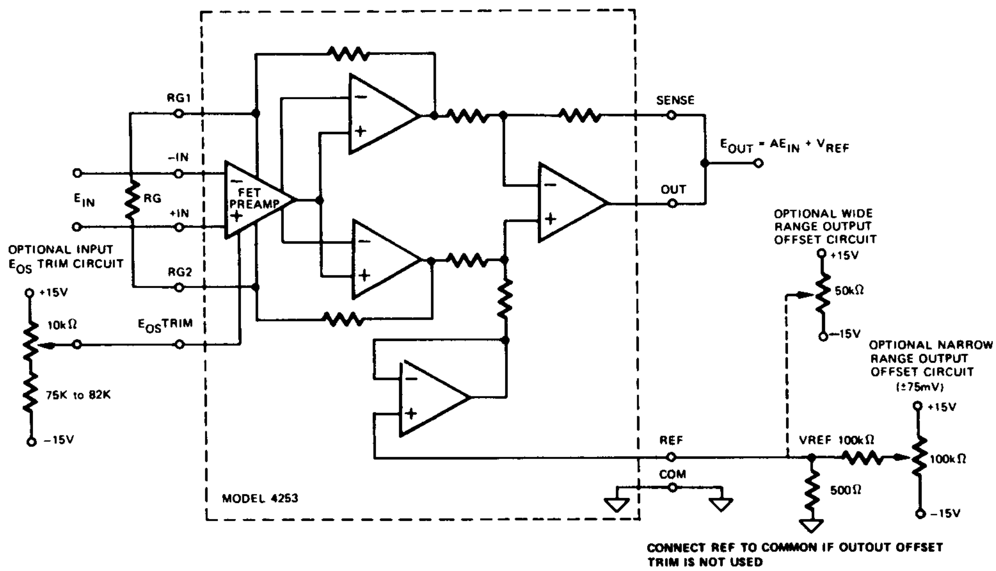


Figure 1. Functional Block Diagram

PROCEDURE FOR OPTIONAL CMR TRIM

For dc Trim:

1. Apply ±10V sine wave (10Hz or less) to 4253 as shown in Figure 2.
2. Adjust dc trimmer for flattest display on oscilloscope.

For ac Trim:

1. Increase frequency of applied CMV signal to frequency of interest. (If not determined, a value between 50Hz and 400Hz is recommended.)
2. Adjust ac trimmer for flattest display on oscilloscope.

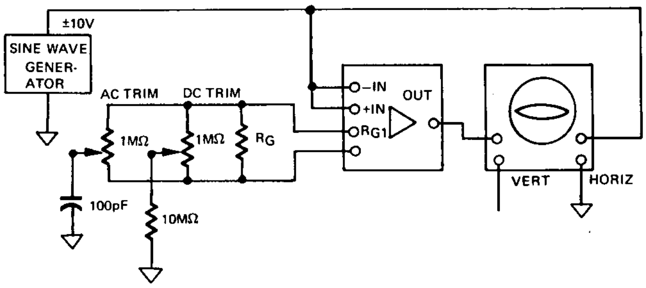


Figure 2. Optional Trim Procedure

UNBALANCED INPUT SOURCE IMPEDANCES

The high input impedance of the Model 4253 ($10^{13}\Omega \parallel 3$ pf) provides superior common mode rejection with high source impedance unbalances. Unbalances of up to 100kΩ do not affect the dc CMR performance. Even with a 60Hz CMV signal, and a 100kΩ unbalance, the CMR of the 4253 will be greater than 80dB.

INPUT BIAS CURRENT

The input bias current of the 4253, although very small, is unipolar and cannot be forgotten. A return path to ground must be provided for both signal inputs.

INPUT/OUTPUT PROTECTION

The model 4253 is fully protected against input voltages up to the supply voltages, and output short-circuits to common. Further, the output will tolerate momentary short circuits to the supply voltages at temperatures below 35°C.

DRIVING LOAD LEADS

Long leads from the output of the 4253 may introduce sufficient series resistance to degrade the signal at the load. To prevent this inaccuracy, connect the "Sense", "output", "Ref", and "Com" leads at the load as shown in Figure 3.

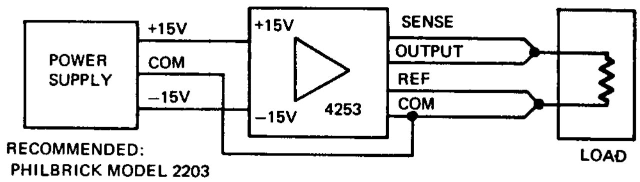


Figure 3. Driving Long Leads

USE OF POWER BOOSTERS

A unity-gain power booster may be used to increase the output current drive capability of the 4253, without degrading other performance characteristics, by connecting it as shown in Figure 4.

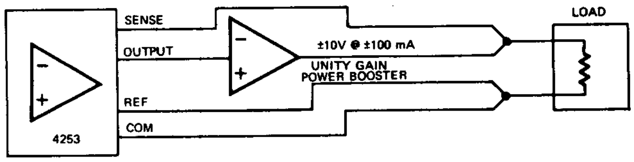


Figure 4. Unity Gain Power Booster

THERMOCOUPLE EFFECTS IN WIRING

Since there are often long leads from the signal transducer to the input of the instrumentation amplifier, there may be one or more copper-to-gold connections in the input wiring. Therefore, it is significant to note that a copper-gold thermocouple produces a junction voltage TC of about 2μV/°C, which is a significant error in comparison to the E_{OS}TC, RTI of the 4253. Use caution!

GROUNDING AND SHIELDING

Inadequate grounding and shielding techniques are the principal source of applications problems with instrumentation amplifiers. Therefore, to obtain optimum circuit performance, it is imperative that sound engineering practices be carefully applied to hold down common mode voltages and to provide adequate input bias current returns. Some specific recommendations are as follows:

a. Ensure that the data acquisition system has a stable ground.

b. Ground the signal circuit at one point only.

c. Signal cable shields should not be used to carry signal currents: they should be connected to ground at only one point, preferably at the signal source.

d. If the signal source operates off ground at some common mode voltage, the signal cable shield should not be grounded: it should be connected to the center tap or the "low" side of the signal source.

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