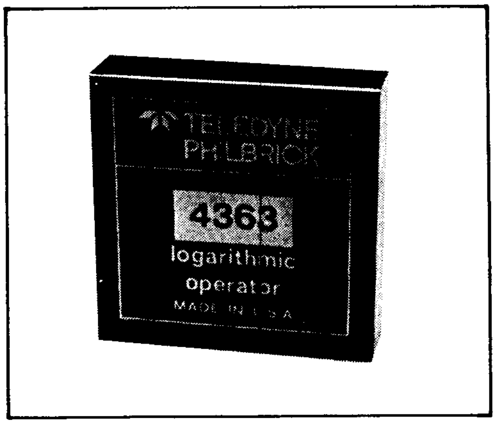
TELEDYNE PHILBRICK

High Performance Temperature Compensated Logarithmic Amplifiers

4362 4363



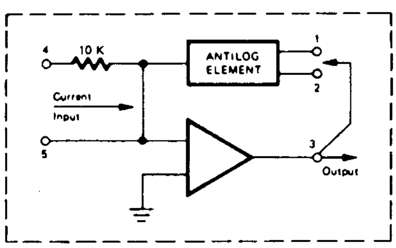
The 4362 and 4363 are high performance, temperature compensated logarithmic amplifiers. 120dB dynamic range, ±3pA max input bias current and ±0.04%FS/°C max full scale drift are some of the inherent features of these versatile devices. Through optional pin strapping, the user has the capability to compute the log of voltages and currents as well as the antilog of voltages at three different sensitivity levels. The 4362 computes the log of positive input currents while the 4363 computes the log of negative input currents. A precision FET amplifier minimizing low level input errors, pretested logging transistors providing log conformity to ±0.5%FS combined with an internal precision reference provide the user with an accurate high performance device.

Applications Information

The 4362 is specifically designed for positive input signals (current or voltage) and the 4363 for negative input signals (current or voltage). For log operation, the input current is applied to pin 5 (summing junction of FET amplifier) and the output (pin 3) to either pin 1 (1V/decade) or pin 2 (2V/decade) or to both pins 1 and 2 (2/3 V/decade). This completes the loop, using the antilog element as the feedback (nonlinear) impedance, thus allowing the output voltage to be proportional to the log of the input current. The output voltage is defined as:

$$V_o = -A \log_{10} \frac{\text{Input Current}}{\text{Reference Current}}$$

The reference current (10^{-5}A) is ideal since it is large compared to the amplifier current errors, yet small enough to define the output voltage maximum as 8V (see Figures 1 & 2). To improve accuracy, the output is designed to swivel each side of zero (Figure 7).



Log Current Operation 4362

Note: For the 4363, the current flows are reversed

FEATURES

- ±0.04%/°C Gain Drift
- Current and Voltage Inputs
- ±0.5%FS Max Log Conformity
- Ultra Low Bias Current
- Output Protection

APPLICATIONS

- Log/Antilog Calculations
- Measuring Circuits for Photo-Semiconductors and Photomultiplier Tubes
- Raising Signals to Arbitrary Powers or Roots
- Linearizing Logarithmic Functions
- Signal Compression to Eliminate Range Switching

TELEDYNE PHILBRICK Allied Drive @ Rte. 128, Dedham, Massachusetts 02026 Tel: (617) 329-1600, TWX: (710) 348-6726, Tlx: 92-4439

SPECIFICATIONS Typical @ 25 °C, ±15 V Supply, unless otherwise indicated

TRANSFER FUNCTIONS FOR 4362 AND 4363

Log of Current:

$$e_{out} = -A\log_{10}\frac{i_{in} - I_o}{I_{ref}} \qquad 10^{-9} < i_{in} < 10^{-3}$$

Log of Voltage:

$$e_{out} = -A\log_{10}\frac{e_{in} - E_{os}}{E_{ref}} \qquad 10^{-3} < e_{in} < 10^{+1}\ V$$

Antilog:

$$e_{out} = E_{ref} \times 10^{-\frac{e_{in}}{A}} \qquad 10^{-3} < e_{out} < 10^{+1}\ V$$

CONSTANTS

A = 1 V/decade ±1% max., 2 V/decade ±2% max., ±0.04%/°C max.
A = 2/3 V per decade ±3%
I_{ref} = 10^{-5} A, ±4% max., ±0.1%/°C max.
E_{ref} = I_{ref} x 10 k, 10^{-1} V nominal
I_{bias} = 0, ±3 pA max., doubles each +10 °C
E_{os} = 0, ±700 μV max., adjustable to zero, ±15 μV/°C max.

DYNAMIC RANGE

Current	120 dB
Voltage	80 dB

LOG CONFORMITY (Referred to Input) (Note 1)

Input Current		Input Voltage
1 nA to 10 nA	±1% max.	
10 nA to 100 μA	±0.5% max.	1 mV to 1 V ±0.5%
100 μA to 1 mA	±1% max.	1 V to 10 V ±1%

RESPONSE

Frequency Response (small signal) ±10% I_{in}

I_{in}	3 dB down at:
10^{-9} A	80 Hz
10^{-6} A	50 kHz
10^{-5} A	60 kHz
10^{-3} A	80 kHz

Rise Time:

I_{in} Increasing	Time	I_{in} Decreasing	Time
10^{-9} to 10^{-8} A	0.5 mSec	10^{-8} to 10^{-9} A	3 mSec
10^{-8} to 10^{-7} A	50 μSec	10^{-7} to 10^{-8} A	300 μSec
10^{-7} to 10^{-6} A	7 μSec	10^{-6} to 10^{-7} A	20 μSec
10^{-6} to 10^{-3} A	7 μSec	10^{-3} to 10^{-6} A	10 μSec

NOISE

Voltage	3 μV rms (160 Hz - 16 kHz)
Current	1.0 pA rms (160 Hz - 16 kHz)

OUTPUT AND POWER

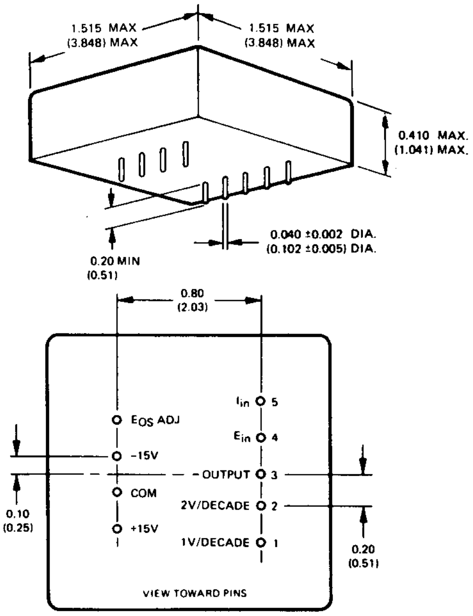
Output	±10 V, 5 mA
Supply	±15 V, regulated ±0.5%, 7 mA max.

PROTECTION No damage from shorting any pin to ground indefinitely or to positive or negative supply for less than 30 seconds.

TEMPERATURE

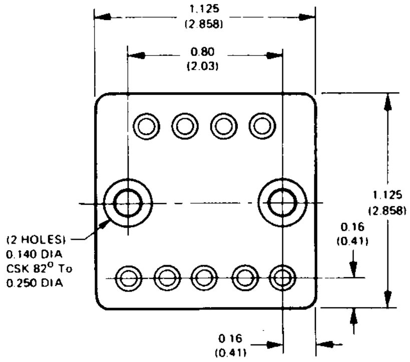
Operating 0 °C to +70 °C Storage -55 °C to +125 °C max.

① Input Signals are positive for 4362 and negative for 4363.



±0.01 Non-cumulative tolerance between pins
±0.02 Tolerance from case edge to center of pins

Optional Socket: Model 6123



BOARD THICKNESS: 0.09 (0.23) ALUM.
OVERALL HEIGHT: 0.68 (1.73)

DIMENSIONS IN PARENTHESES ARE EXPRESSED IN CENTIMETERS

The sensitivity multiplier "A" in the formula has a value of 2, 1, or 2/3 volts change in output per decade of input current change.

A minus sign is associated with the constant "A" to comply with the accepted convention denoting reversal of signal polarity through the device. A positive *change* in input voltage (or current) produces a negative *change* in output voltage and vice versa.

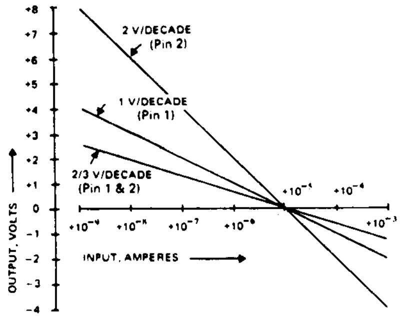


Figure 1. Model 4362 Log of Current (Positive Signal)

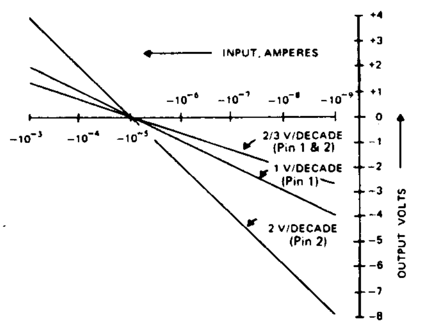


Figure 2. Model 4363 Log of Current (Negative Signal)

LOG OF VOLTAGE

For log voltage operation, the input voltage is simply converted to be *the* input current; from there on operation is identical to that just described under "Log of Currents."

Since the summing point (terminal 5) is a virtual ground under all operating conditions, a suitable resistor between it and the voltage signal source will perform the conversion. For convenience, a precise 10kΩ resistor, internally connected to the summing point, is provided at terminal 4. As shown in Figs. 3 & 4, this value sets full scale voltage at 10V, since it produces 1mA, rated full scale input current. Note that it also sets the value of Reference Voltage, E_{ref}, at 100mV, i.e., $I_{ref} \times 10k\Omega$, since I_{ref} of 10^{-5}A is internally provided.

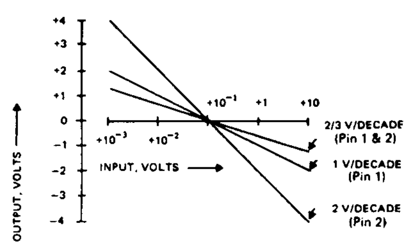


Figure 3. Model 4362 Log of Voltage (Positive Signal)

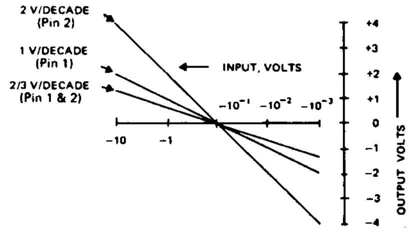
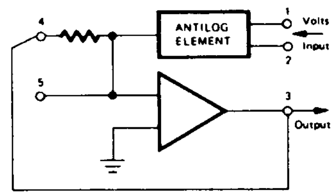


Figure 4. Model 4363 Log of Voltage (Negative Signal)

ANTILOG OF VOLTAGE

For antilog voltage operation, the input signal is applied to the antilog element at terminal 1 (for 1 decade/volt sensitivity), or to terminal 2 (for 0.5 decade/volt sensitivity). The resulting current at the summing point is converted to voltage by the built-in 10kΩ feedback resistor, when terminals 3 & 4 are reconnected together.



Antilog Voltage Operation 4362, 4363

Figures 5 & 6 show the output voltage to be expected from each log module, when connected to find the antilogarithm of a voltage.

In the 4362, I_{ref} (10^{-5}A) flows from the summing point when E_{in} = zero. The operational amplifier output must supply this current through the feedback resistor, and the value of positive output required is the reference voltage. Use of a 10kΩ resistor then defines E_{ref} as 100 millivolts, as shown in Figure 5. The action of the 4363 is the same, however, the currents are reversed, as shown in Figure 6. Other values of feedback resistors produce other values of E_{ref}.

The output voltage with either 4362 or 4363 equals:

$$e_{out} = -E_{ref} \times 10^{\frac{e_{in}}{-A}} \pm E_{os}$$

in which E_{ref} refers to the magnitude of the Reference Voltage. The negative sign denotes the reversal of polarity from input to output. See Figures 5 & 6. The resistance seen looking into terminal 2 is 5.7kΩ.

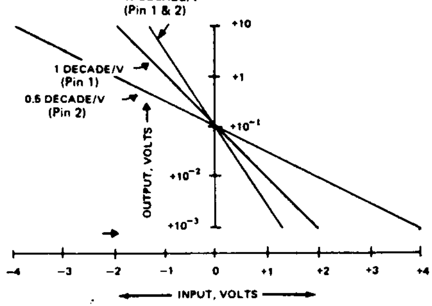


Figure 5. Model 4362 Antilog of Voltage (Positive Output)

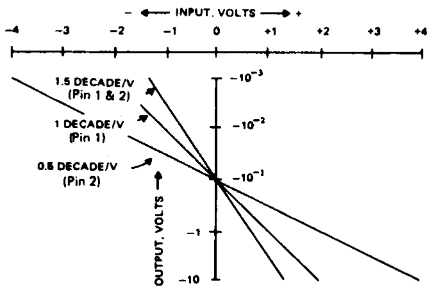


Figure 6. Model 4363 Antilog of Voltage (Negative Output)

OFFSET TRIMMING (Optional)

When logging voltage, the input current can no longer be specified as the independent variable, it is now determined by the *difference* between E_{in} and E_{OS}, the offset error voltage apparent at the summing point. Although E_{OS} can be trimmed essentially to zero, it is never perfect. A ½% error due solely to this cause *alone*, when operating over a 4 decade *range*, implies that E_{OS} must be less than ½% of 1mV (5μV).

When used in the log mode input, offset voltage (E_{OS}) can be trimmed for improved accuracy. Since trimming the offset voltage to zero will cause the device to saturate, the best compromise is as follows: 1. connect a high resolution, 100kΩ pot across the ±supplies, with the center arm connected to the E_{OS} ADJ pin, 2. with appropriate scale factor pin connected to the OUT pin, adjust the trim pot for an output voltage of more than 4x scale factor (volts). This gives an offset of less than 10μV.

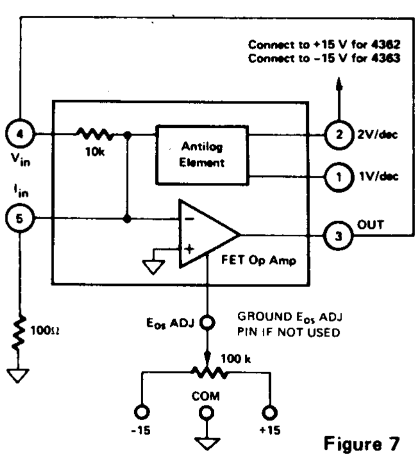


Figure 7

A second method of trimming can be used which is inherently more accurate, although it may prove difficult if the unit is already connected in the log mode. It is as follows: 1. "turn off" inherently generated reference current flowing into the summing point by connecting terminal 2 to the appropriate supply voltage (see Figure 7), 2. for either model, connect terminal 3 to 4 to use the internal feedback resistor. Between terminals 5 and COM connect a 100Ω resistor. The output now consists of the offset error voltage, E_{OS}, amplified by a factor of 101, and is zeroed by the trim pot.

Since the E_{OS} T.C. can be ±15μV/°C, the trimming should be performed after a warm-up to the ambient temperature in which the module will be used. This is particularly critical for the log mode trimming when the offset is trimmed as in procedure No. 1.

OTHER REFERENCE CURRENT AND VOLTAGES

For a reference current other than 10^{-5}A or a reference voltage other than 10^{-1}V, insert a constant current into Pin 1 or Pin 2 (whichever is not in use). Each 350μA of current changes the reference by one decade. Note: a positive current decreases the algebraic value of the reference for the 4362 (and a negative current for the 4363). The input current must not be allowed to exceed 1mA, and the output must not be required to exceed ±10V. For easier computation, the input impedance at Pin 1 is approximately 2.85kΩ, at Pin 2 is approximately 5.7kΩ.

Logging of other full scale voltages is readily done by use of an external resistor connected between the source and terminal 5, the summing point, to convert the voltage to current. A kilovolt full scale input is perfectly practical using a 1 megohm resistor, but prudence demands fault protection, such as a pair of low leakage diodes back-to-back connected between the summing point, "I_{in}," and the "COM" terminal for the power supply.

Changing the scale factor, or sensitivity, A, is done at the input of the antilog element. Note first the dimensions of the constant, A, is of the nature of volts/decade, then note that the resistance looking into terminal 2 is 5.7kΩ (2V/decade) and into terminal 1 is 2.85kΩ (1V/decade). To obtain any other value for A, simply add resistance to say terminal 1, to bring up the total to approximately 2.85kΩ for each volt desired to represent a decade change in the input current. Thus for 3V/decade, add 5.7kΩ (approx.) to terminal 1. This circuit technique can be used to take the square or cube root of a number; refer to Application Notes.

A more convenient way of scaling, either up or down, as well as biasing the output (moving to its apparent zero) is to add an other operational amplifier (or attenuator) stage following the logger.

RTI AND RTO ERRORS

It is useful to remember when working with logarithmic amplifiers that a given output dc error produces a fixed percent error referred to the input, and that the scale factor directly relates these RTI and RTO errors. Specifically, a 0.1% RTI error corresponds to a 0.43mV RTO error at a scale factor of 1 volt/decade (and a 0.86mV RTO error at 2 volt/decade).

ERROR ANALYSIS

Preliminary to discussion of log device errors, mention of the ideal device characteristics, Figures 1 thru 6, is warranted. Note that, as presented on semi-log co-ordinates, the equation of the ideal is completely described by 2 constants, namely, slope ("A"), and intercept ("I_{ref}"). More specifically, "A" is numerically and dimensionally expressed as volts/decade. "I_{ref}" is simply that precise value of current at which the antilog element has its input, terminal 1, driven to exactly zero volts (by the output of the op amp, when logging current or voltage).

The numerical values of "A" or "I_{ref}" actually observed may not be precisely what the user wanted, but the relationship of output to input is still perfectly logarithmic-ideal. Another category of error, a catch-all, is required for those deviations from an ideal log relationship, generally referred to as "nonlinear" errors or, "log conformity" error, etc.

Thus we have 3 categories in which to assess errors:

1. Slope (A)
2. Intercept (I_{ref})
3. Log Conformity (nonlinearity %)

Fortunately, once trimmed, these log devices exhibit insignificant "nonlinear" errors in the middle 4 decades. In the lowest and in the highest decade, errors which are irreducible begin to appear and are the basis of specifications for accuracy in the current logging.

The effect of offset voltage error, E_{os}, is felt in 2 categories, intercept and log conformity. Intercept, i.e., the voltage at terminal 1 corresponding to I_{ref}, will shift from zero volts by approximately a factor of 17 times E_{os} (34 X E_{os} at terminal 2). Note, that is the output as a logger, and the input as an antilogger. In the case of log voltage operation, the actual input current is determined by $E_{in}-E_{os}$, hence E_{os} will produce a nonlinear error felt only at the lowest decade of input.

Input error current, I_o, internally generated into the summing point is negligible at room temperature (1pA typ.) but may become significant at elevated case temperatures. Since it is simply a fixed, spurious input current, its sole effect is a nonlinear error at the lowest decade of input. Although such error can be compensated out by an equal and and opposite current into the summing point, the difficulties of doing so are too great to consider practical.

Mention should be made of the need for shielding and guarding to prevent external stray currents from leaking into the summing point terminal. For lowest input level applications use of the No. 6123 socket plus careful RF (and 60Hz) shielding is recommended.*

APPLICATIONS ASSISTANCE

Available upon request from our Literature Department are three Teledyne Philbrick Application Notes on loggers:

AN-12: Designers Guide to Logarithmic Amplifiers

AN-14: 4350/51, 4362/63 Application Notes

AN-15: How to Specify Parameters of Nonlinear Circuits

AN-27: Logarithmic Amplifiers and Operators Parameter Definition and Measurement

*Where minimum input signal is 10^{-7} or larger, such as voltage logging, the NSK-20 socket is adequate.