

# 1MHz High Performance, Low Drift Voltage to Frequency Converter

The 4719 high performance, low drift voltage to frequency converter provides a 1Hz to 1MHz output pulse train from a  $\pm 10\mu\text{V}$  to  $\pm 10\text{V}$  input signal. Twenty percent overrange, 20 bit dynamic range, and low drift, as well as voltage and current inputs are features that allow this versatile device to perform in a wide range of applications. Where increased temperature stability is required, the 4719-01 is available with a guaranteed  $\pm 25\text{ppm}$  of FS/ $^{\circ}\text{C}$  full scale drift over the  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range. Applications include data acquisition, data transmission, frequency multiplication and infinite hold time integration. As a current to frequency converter, the 4719 resolves currents as low as 1nA allowing operation with full scale input voltages from less than 250mV to greater than 100 volts.

## Applications Information

This voltage to frequency converter is factory trimmed to a zero and full scale accuracy of better than  $\pm 0.02\%$  FS. Thus, for most positive voltage input applications, it is connected as shown in Figure 1 without the addition of trim components. This produces a TTL compatible output pulse with nominal width equal to  $\frac{1}{2}$  the period of device full scale frequency.

When greater accuracy is required, input offset voltage ( $E_{OS}$ ) and full scale (FS) output frequency are trimmed with external potentiometers as shown in Figure 2.

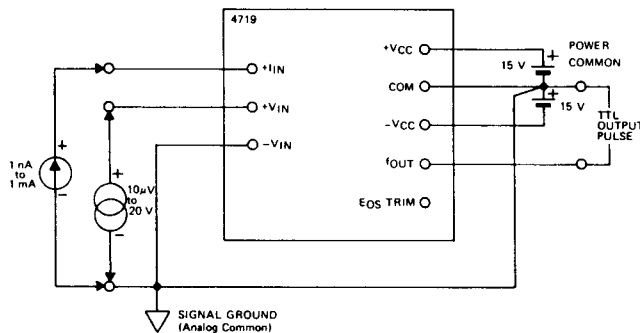
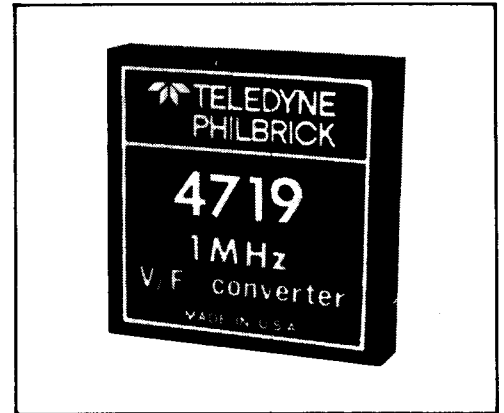


Figure 1. Positive Input Signals

# 4719



## FEATURES

- 1Hz to 1MHz Frequency Range
- $\pm 0.02\%$  FS Max Nonlinearity
- $\pm 25\text{ppm}$  of FS/ $^{\circ}\text{C}$  Max Full Scale Drift
- 20 Bit Resolution
- Positive and Negative Voltage Inputs
- Low Cost

## APPLICATIONS

- Process Transducers
- Digital Frequency Synthesis
- FM Telemetry
- Servo Loops

SPECIFICATIONS @ +25 °C, ±V<sub>CC</sub>, ±15 V (unless otherwise indicated)

	TYPICAL	GUARANTEED	
<b>FULL SCALE (FS)</b>			
Ideal Transfer Function	---	$f_{out} = \frac{(V_{in}) (1 \text{ MHz})}{10 \text{ V}} = \frac{(I_{in}) (1 \text{ MHz})}{1 \text{ mA}}$	
Full Scale Factor (Input for 1 MHz Out)			
+V <sub>in</sub> , -V <sub>in</sub> (factory trimmed)	---	9.9 V ±0.5% trimmable to 10.00	
+I <sub>in</sub>	---	1 mA ±25%	
Range (for specified nonlinearity) ①			
+V <sub>in</sub> Terminal	+10 μV to +12 V	+100 μV to +11 V	
-V <sub>in</sub> Terminal	-10 μV to [-V <sub>CC</sub> +4.9 V]	-100 μV to [-V <sub>CC</sub> +4.9 V]	
+I <sub>in</sub> Terminal	1 nA to 2 mA	10 nA to 1 mA (±25%)	
Differential [(+V <sub>in</sub> ) - (-V <sub>in</sub> )] ②	±12 V	±11 V, (±V <sub>CC</sub> fault)	
Over Range Max., +V <sub>in</sub> , (-V <sub>in</sub> = 0)	+V <sub>in</sub> = 20 V, f <sub>out</sub> = 2 MHz	+V <sub>in</sub> = +15 V, f <sub>out</sub> = 1.5 MHz	
Dynamic Range	126 dB	100 dB	
Common Mode Voltage ②	+12 V, -11 V	±10 V	
CMRR, CMV = ±10 V	80 dB	60 dB for 100 Hz ≤ f <sub>out</sub> ≤ 1 MHz	
<b>NONLINEARITY ± % FS</b>			
+V <sub>in</sub> (+10 μV to +11 V)	.01	.02	
-V <sub>in</sub> (-10 μV to -11 V)	.03	.05	
+I <sub>in</sub> (10 nA to 1.1 mA)	.01	.02	
+V <sub>in</sub> (+10 μV to +11.0 V) ③ ④	.01	.02	
-V <sub>in</sub> (-100 μV to -V <sub>CC</sub> +4.9 V) ④	.03	.05	
+V <sub>in</sub> (+10 μV to +15 V) (overrange)	.03	.05	
<b>INPUT</b>			
Zero Offset Voltage, Initial Untrimmed	±2 mV	±5 mV (trimmable to zero)	
Impedance @ +V <sub>in</sub>	---	10 KΩ ±25%	
Impedance @ -V <sub>in</sub>	100 Meg Ω	10 Meg Ω	
Impedance @ +I <sub>in</sub> (op amp summing point)	Virtual Ground	< 0.1 Ω	
<b>STABILITY OF FULL SCALE FACTOR</b>			
Temperature Coefficient (+V <sub>in</sub> , -V <sub>in</sub> ) ±PPM/°C ④	25	4719-01	4719 25
Temperature Coefficient (+I <sub>in</sub> ) PPM/°C ④	20	20	---
Power Supply Sensitivity ±PPM/% Δ V <sub>CC</sub> ④	10	10	20 20
Drift: Per Day/Per Month ±PPM	10/30	10/30	---
Warm Up Time to .01%/0.02% of FS	1 s/100 s	1 s/100 s	---
<b>STABILITY OF ZERO OFFSET VOLTAGE</b>			
Temperature Coefficient ± μV/°C ④	±12	±25	
Power Supply Sensitivity ± μV/% Δ V <sub>CC</sub> ④	5	10	
Drift: Per Day/Per Month	20 μV/60 μV	---	
<b>RESPONSE</b>			
Settling Time to .01% for FS step input	---	1 to 2 pulses of new frequency +5 μsec	
Overload Recovery (V <sub>in</sub> = +50 to V <sub>in</sub> = +10) or (I <sub>in</sub> = 5 mA to I <sub>in</sub> = 1 mA)	.14 msec	.1 msec	
<b>OUTPUT WAVEFORM</b>			
High (positive logic "1")	---	TTL compatible	
Low (positive logic "0")	---	+2.4 V to +5 V (up to 10 TTL Load)	
Pulse Width	---	≤0.4 V @ -16 mA Sink Current	
Source Impedance (High)	---	.15 μsec to .35 μsec	
		680 Ω ±20%	
<b>POWER REQUIREMENT</b>			
Voltage Range (±V <sub>CC</sub> )	±8.0 V to ±18 V	±9 V to ±18 V	
Voltage Asymmetry (Δ between  +V <sub>CC</sub>   &  -V <sub>CC</sub>  )	---	±2 V	
Current (±I <sub>CC</sub> ) @ V <sub>CC</sub> = ±15 V	±35 mA	±45 mA	
<b>ENVIRONMENT/RELIABILITY</b>			
Operating Temperature	---	-25 °C to +85 °C	
Storage Temperature Absolute Max.	---	-55 °C to +125 °C	

Input Protection: All voltage inputs may be shorted to ±V<sub>CC</sub> indefinitely without damage, I<sub>in</sub> must be limited to 5 mA.  
Output Protection: May be shorted to ground indefinitely; to +V<sub>CC</sub> for 5 seconds.

## NOTES

- ① After trim @ 1 KHz and 1 MHz
- ② See Figure 6D for definition
- ③ Constant voltage at Zero trim pin
- ④ Temperature Coefficients measured from -25 °C to +85 °C
- ⑤ Measurement, made for ±V<sub>CC</sub> = ±9 V to ±18 V
- ⑥ Over -25 °C to +85 °C

1. Apply 10 mV between R1 and Signal Ground. Adjust R2 for  $f_{out} = 1$  kHz. (See Figure 2).
  2. Apply 10 V between R1 and Signal Ground. Adjust R1 for  $f_{out} = 1$  MHz.
  3. Repeat (1) and (2) for precise Zero & Full Scale set.
- Note: All fixed and variable trim components should have temperature coefficients similar to that of the V to F being used, e.g., they should be wire wound, metal film or cermet.

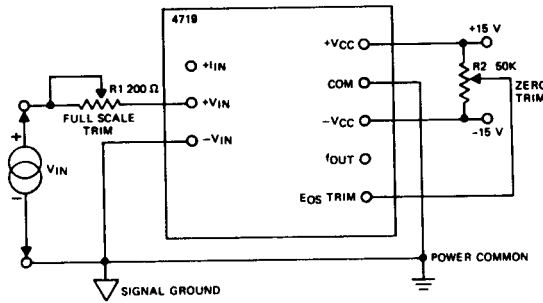


Figure 2. Zero & Full Scale Trim Positive Voltage Input

**Negative Input Signals (Input to  $-V_{in}$  Pin)**

The 4719 can operate with negative input voltages as great as  $-10$  V applied to the  $-V_{in}$  pin as shown in Figure 4B. This negative ten volt signal will produce a Full Scale Output Frequency of 1 MHz. To obtain specified Full Scale output frequency for an input voltage of less than plus or minus 10 volts, see **FULL SCALE FACTOR CHANGE**. It should be noted that input impedance at the  $-V_{in}$  pin is typically greater than 10 Meg ohm.

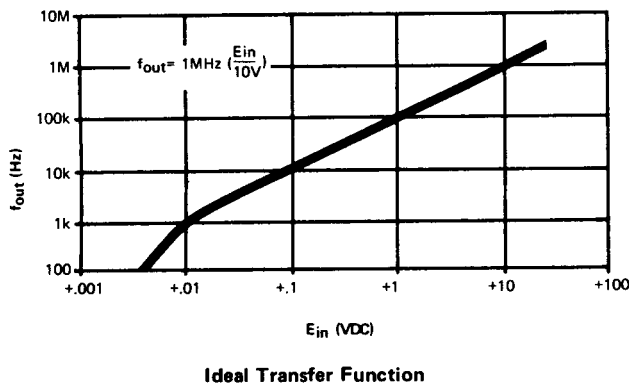
**Zero & Full Scale Trim (Input to  $-V_{in}$  Pin)**

Zero Trim is performed with R2 as shown in Figure 2. For Full Scale Trim, connect R1 between  $+V_{in}$  and Signal Ground as shown in Figure 4B.

Follow the Trim Procedure for signals at the  $+V_{in}$  pin.

**Current Input (Signal to  $+I_{in}$  Pin)**

The Full Scale Current Sensitivity  $I_{FS}$  of each V to F model has a tolerance of about  $\pm 25\%$ . The exact  $f_{FS}$  may be set using the circuit of Figure 5A.



**THEORY OF OPERATION**

To take maximum advantage of V to F versatility, a functional block diagram (Figure 3) and theory of operation is provided. With this information, input and output circuitry are easily modified to handle virtually any signal or load.

The V to F is a free running (astable) voltage controlled multivibrator (see Figure 3). The effective currents from the three inputs (A, B, & C) are summed at the minus input of op amp A1. A1 and transistor Q1 form a precision current pump, producing current I from the collector of Q1, which is a linear function of the A1 input currents. Current I charges capacitor C at a rate which is a precise linear function of the V to F input.

When the voltage impressed on C (due to I) reaches a fixed precision threshold, the Schmitt-Trigger output changes state and triggers the one-shot (monostable) multivibrator, which in turn produces a constant width output pulse. This pulse performs two functions. Amplified by Q2, it is the output of the V to F and it functionally activates the Precision Charge Dispenser (PCD). The PCD discharges C to the same reference level every time an output pulse is produced. Thus, capacitor C is repeatedly charged between two precise voltages at a rate which is a linear function of the input signal, producing the waveforms shown in the timing diagram, Figure 7. That is, the rate of charging C, (the repetition rate of charging C and thus the output frequency) are functions of the V to F voltage and/or current inputs.

**TRIM THEORY**

The V to F input circuit Zero and Full Scale trim techniques are based on the input circuit amp (A1, Figure 3) and the user may treat the input as such within certain limits. No combination of signals may be applied to the inputs which will drive the A1 output positive. That is, a frequency output will not result if the total current into the positive inputs (A1, summing point) becomes negative with respect to the negative input. If this occurs, D1 will become forward biased, Q1 cut off, I becomes zero, and  $f_{out}$  becomes zero. The inherent current Full Scale Factor has a tolerance of  $\pm 25\%$  to give specified Full Scale frequency out. Factory trims the full scale  $\pm V_{in}$  to within 0.5%.

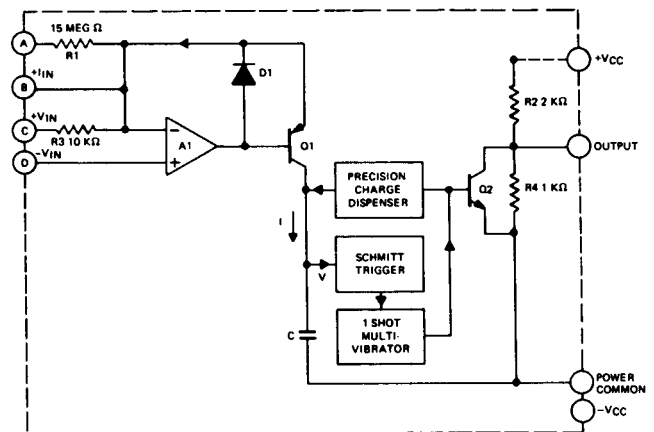


Figure 3. V to F Simplified Block Diagram

**FULL SCALE FACTOR CHANGE**

The Specified V to F Full Scale Factor is  $9.9 \text{ V} \pm 0.05 \text{ V}$  to produce Full Scale Frequency out. Many applications require FS  $f_{out}$  for other (larger or smaller) Full Scale input signals and polarities. Figures 4A through 4E illustrate how to operate these V to F's with such signal levels.

**Magnitude of  $V_{in} > 10 \text{ Volts}$**

The 4719 can be operated with input voltages greater than +10 V by connecting a fixed resistor and trim potentiometer in series with the + voltage input (see Figure 4A). For voltages more negative than -10 V, the attenuator network of Figure 4B performs well. Zero Trim and other adjustments remain the same as for Figure 2.

If the full scale input voltage is between  $+10 \mu\text{V}$  and  $+100 \text{ mV}$  the full scale output is set by using the + current input terminal with a series resistor as shown in Figure 4C. The only effect will be to reduce dynamic range since the minimum input voltage does not change from  $10 \mu\text{V}$ . To keep a 120 dB dynamic range, use a circuit similar to Figure 4A. When the Full Scale Input Signal is between -0.1 volts and +0.1 volts, a low drift amplifier such as the TP 1703 should be used to raise the signal to 10 V. See Figure 4D.

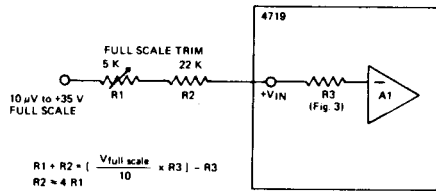


Figure 4A. Full Scale  $+V_{IN}$  Greater than +10 V

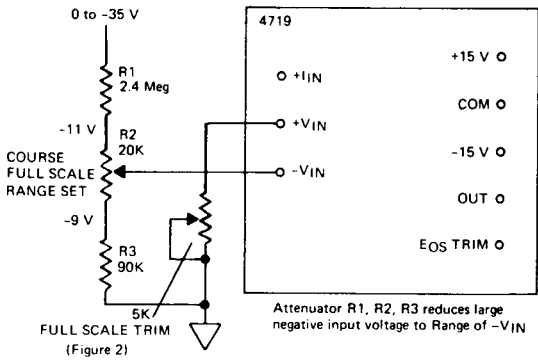


Figure 4B. Full Scale Input Voltage More Negative than -10 V

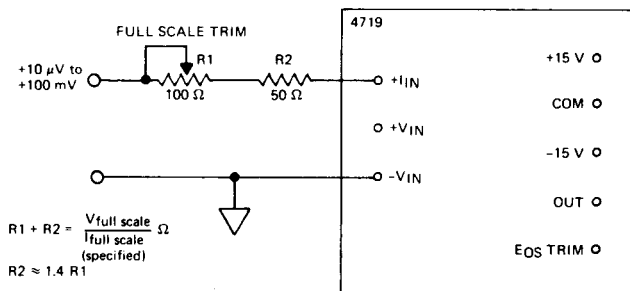


Figure 4C. Full Scale Input Between  $\approx +10 \mu\text{V}$  and  $+100 \text{ mV}$

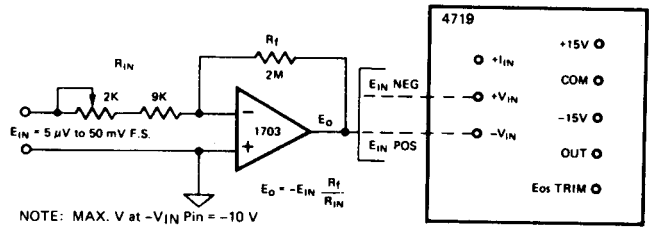


Figure 4D. Full Scale Input Voltage Between -1 V and +1 V

**Reduce Full Scale  $f_{out}$  Below Specified FS  $f_{out}$**

In some applications, a Full Scale output frequency of less than specified Full Scale is required when the input signal is 10 volts or greater. The circuits of Figures 4 and 5 which show attenuation of the input signal to 10 volts can be used to decrease the Full Scale input signal below 10 V and, therefore, decreases Full Scale  $f_{out}$ .

To maximize use of the dynamic range, the input signal is conditioned to +10 V or -10 V and a binary or BCD frequency divider (counter) is connected to the output. Any TTL or CMOS device may be used, from a simple divide by 10 unit to the CMOS CD4059, which can divide by any number from 3 to 15,999.

If, for example, the 4719 FS output is set at 1 MHz, as shown in Figure 4E, counter output will be 100 kHz while the minimum output frequency will be 100 mHz.

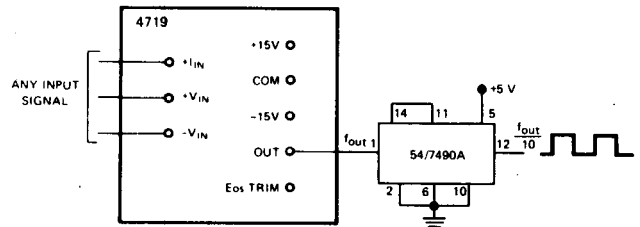


Figure 4E. Full Scale Output Less Than Specified When  $V_{IN}$  is Equal To Or Greater Than 10 V

**Full Scale Input Current Greater Than Specified**

If the full scale input current is greater than +1 mA, the "current splitter" circuit of Figure 5A is used. As noted in Figure 5A, the voltage developed at the wiper of the potentiometer must be less than the compliance voltage of the current source. A negative input current is conditioned by passing it through a resistor connected between  $-V_{in}$  and signal common and thus producing a negative voltage. (Trim with pot between  $+V_{in}$  and common.) The compliance voltage of the current source must be greater than the maximum voltage developed across the resistor.

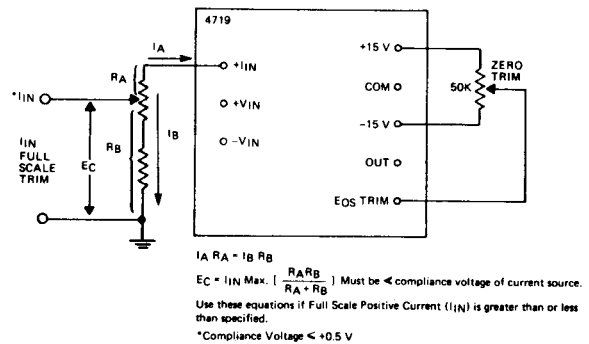


Figure 5A. Zero & Full Scale Trim for Positive Input Currents

The best way to **CONDITION CURRENT SIGNALS** is with the classic current to voltage converter circuit shown in Figure 5B. With this circuit and the "right" amplifier, virtually any current (even femtoamps) will provide a positive or negative full scale input with no compliance voltage problem.

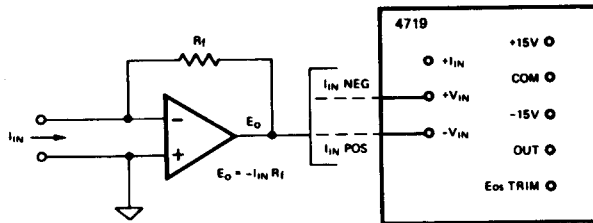


Figure 5B. Full Scale Input Currents Negative Of Less Than 1 mA

**OPERATION WITH BIPOLAR, FAST, or NON-ZERO BASED INPUT SIGNALS – "OFFSETTING"**

Many V to F applications require operation with bipolar input signals (e.g. -5 V to +5 V). In other applications the input signal is changing rapidly (e.g. ±1 V @ 100 kHz). In still others the input signal does not pass through zero (e.g. +6 V to +8 V).

Such signals cannot be handled by V to F's when connected as illustrated in Figures 1 through 5. However, their versatile op amp input circuit is easily adaptable to these signals through the technique of **OFFSETTING**. It is implemented by the application of a fixed **OFFSET** signal to one of the three V to F inputs, usually such as to produce an output or **OFFSET** frequency when the input signal of interest is zero. Essentially the **OFFSET** voltage or current is algebraically added to the signal of interest at the op amp summing point. The effective input resistor for the plus and minus V<sub>in</sub> pins is R3 in Figure 3. A different **OFFSET** technique is required for each of these three types of input signals, therefore, they are described separately.

$$R1 + R2 = \frac{V_{CC}}{I_{OFFSET}} \quad I_{OFFSET} = \frac{V_{OFFSET}}{10V} \times I_{FULL\ SCALE}$$

$$R1 + R2 \text{ in } K\Omega = \frac{15}{0.5 \text{ mA} \pm 25\%} \quad = \frac{5}{10} \times 1 \text{ mA} \pm 25\%$$

$$= 0.5 \text{ mA} \pm 25\%$$

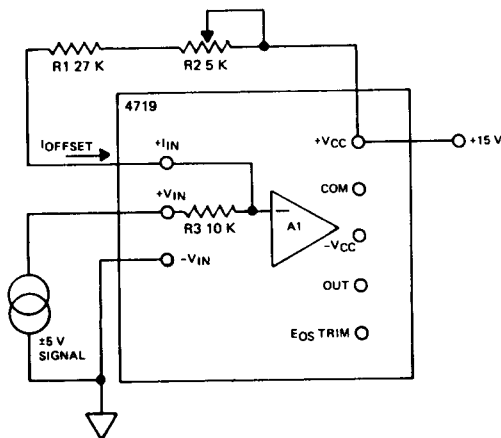


Figure 6 A. V to F With +5 V Offset Allows Operation With Bipolar ±5 V Input Signal

**Operation With Bipolar Input Signals**

A ±5 V signal connected to the +V<sub>in</sub> pin of a 4719 as shown in Figure 2 will produce no output from -5 V to 0 V and 0 to 500 kHz out from 0 V to +5 V<sub>in</sub>. Essentially an **OFFSET** of +5 V (½ Full Scale) must be added to the +5 V input voltage to produce 1 Hz out for +5 V<sub>in</sub>, 500 kHz out for 0 V in and 1 MHz out for +5 V<sub>in</sub>. This may be accomplished as shown in Figure 6A by injecting an offset current into the +I<sub>in</sub> pin through R1 and R2. This is the equivalent of connecting a resistor, with the same value as the +V<sub>in</sub> input resistor (10 K), to +5 V.

**Operation With Non-Zero Based Signals (Figure 6B)**

When the signal of interest is a small changing voltage impressed on a fixed DC voltage, the +V<sub>in</sub> pin is offset to eliminate the fixed voltage while the signal is applied to the +I<sub>in</sub> pin to provide a scale factor increase. For example, in Figure 6B a 2 V signal is impressed on a fixed +15 V. The +15 V is offset to zero by summing it through R1 and R2 at the op amp +I<sub>in</sub> pin with -15 V from -V<sub>CC</sub> through the 10 K +V<sub>in</sub> input resistor, R1 and R2 reduce the scale factor so the 2 volt signal provides a full 1 MHz out from the 4719. The 50 K offset trim pot is used to set the minimum f<sub>out</sub>, while R1 sets maximum f<sub>out</sub>.

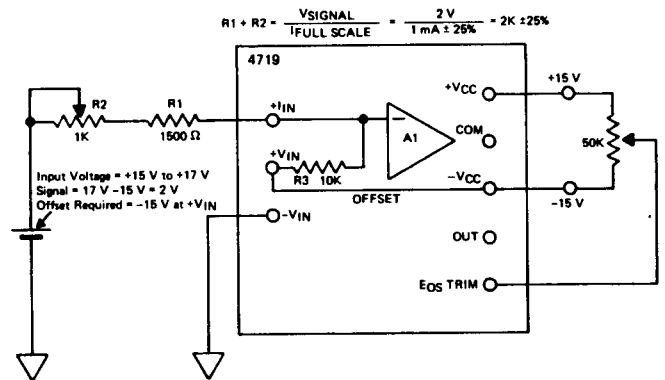


Figure 6B. V to F With -15 V Offset Allows Operation With Small (2 V) Signal Impressed on Larger DC Voltage (+15 V)

**Operation With Fast Signals (FM Modulation)**

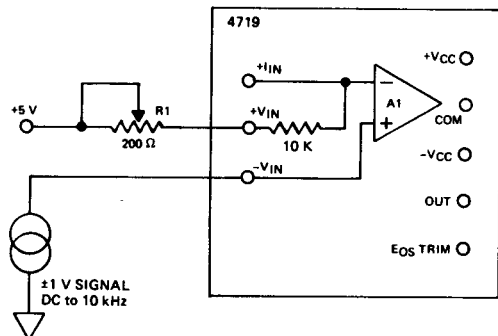
A basic V to F application requiring operation from DC to high frequency input signals (for example, a fiber optic FM data link with response from DC to 10 kHz). To accurately handle this signal the output of the V to F must be able to change much faster than the input. The basic response time of a V to F is one period of the new frequency plus approximately 5 μsec. For example, if the input of a 4719, 1 MHz V to F is changed one volt from 1.01 volts to 0.01 volts the new frequency is 1 kHz and response time is 1/1 kHz + 5 μsec or ≈ 1 msec. When the input changes from 11 volts to 10 volts the new frequency is 1 MHz and response time is ≈ 6 μsec. If the system is to accurately follow a 10 kHz input sine wave, V to F response must be less than 1/10 the period of the signal of interest. This is accomplished as shown in Figure 6C by offsetting the V to F output to .5 MHz with +5 V at the +V<sub>in</sub> pin and connecting the ±1 V signal to the -V<sub>in</sub> pin.

**Operation With Differential Input Signals (4719)**

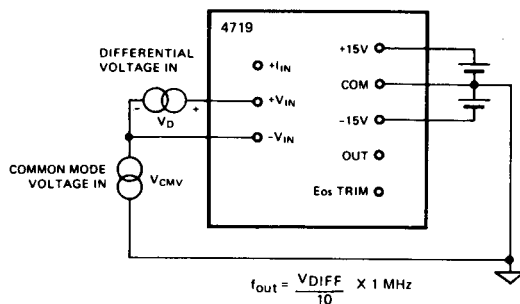
The +V<sub>in</sub> and -V<sub>in</sub> pins of the 4719 represent a differential input capable of accepting a ±11 V signal from a balanced line or bridge transducer and rejecting any common mode voltage. This ability often eliminates the need for a differential amplifier. However, to effectively use this pair of input terminals differentially, several simple conventions (definitions) must be observed as illustrated in Figure 6D.

1. Common Mode Voltage (CMV) is defined as the voltage between ±V<sub>CC</sub> common and the negative V<sub>in</sub> pin.
2. The positive V<sub>in</sub> pin must always be positive with respect to the negative V<sub>in</sub> pin.
3. CMV Range is typically +12, -11 V.
4. The differential (floating, balanced) signal source must be returned to ±V<sub>CC</sub> common through a resistance and must not create voltages which exceed the limits set by 1, 2, and 3.

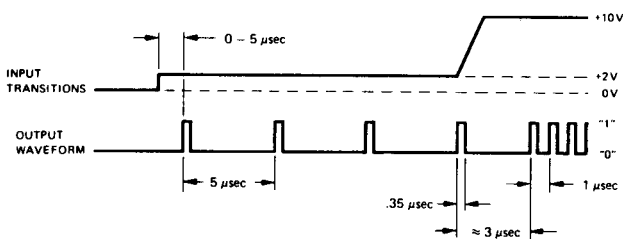
$$f_{out} = \frac{(+V_{in}) - (-V_{in}) \times 1 \text{ MHz}}{10 \text{ V}}$$



**Figure 6C. V to F With Offset (+5 V) To Positive Fast Response (10 kHz)**



**Figure 6D. Definition of Differential & Common Mode Voltage**



**Figure 7. V to F Output Waveform & Timing**

**OUTPUT CIRCUIT**

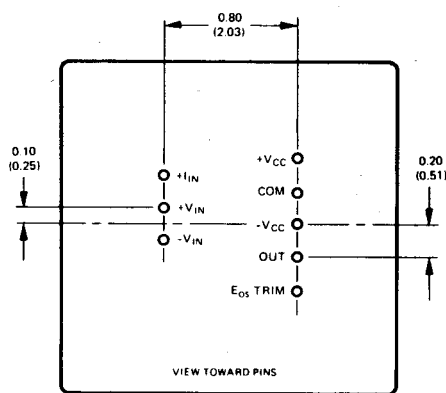
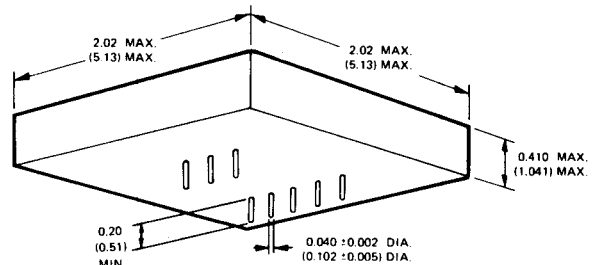
**Wave Form**

The output circuit of the V to F (see Figure 3) is designed to drive 10 TTL loads. Output pulse amplitude of the 4719 may be increased by shunting R2, or decreased by shunting R4. This will also increase rise time and the ability to drive a capacitive load.

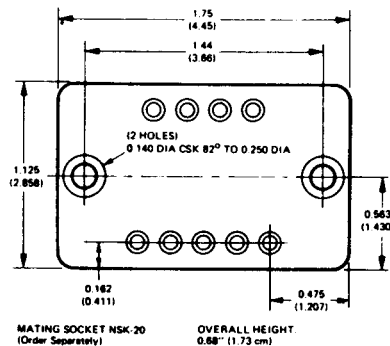
Figure 7 illustrates typical output pulse shape, timing, and waveform.

**Protection**

The output of these V to F's may be shorted to common indefinitely, and to +V<sub>CC</sub> for several microseconds, but they must *never* be connected to -V<sub>CC</sub> or failure will result.



±0.01 Non-cumulative tolerance between pins  
±0.02 Tolerance from case edge to center of pin  
Dimensions in parentheses are expressed in centimeters



MATING SOCKET NSK-20 (Order Separately)

OVERALL HEIGHT: 0.88" (1.73 cm)

**Figure 8. Mechanical Dimensions**

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Allied Drive @ Rte. 128, Dedham, Massachusetts 02026  
Tel: (617) 329-1600, TWX: (710) 348-6726, Tlx: 92-4439