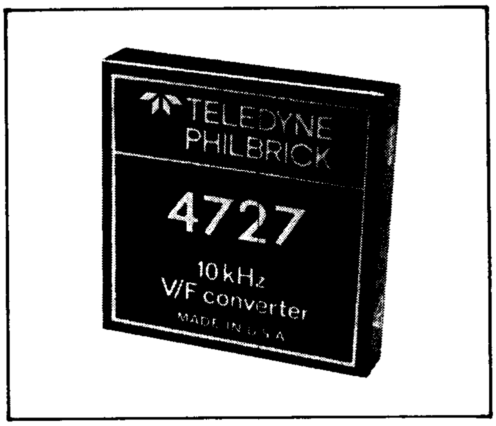
TELEDYNE PHILBRICK

10kHz Precision, Low Drift Voltage to Frequency Converter

4727

The 4727 is a precision, low drift voltage to frequency converter that is capable of producing a 0.01Hz to 10kHz output pulse train from a ± 10μV to ± 10V input signal. Thirty percent overrange, 120dB of dynamic range and the ability to handle voltage and current input signals are some of the features incorporated into this high performance device. The 4727's ± 0.001%FS nonlinearity is equivalent to 16 bit end point linearity, while differential nonlinearity and dynamic range approach 20 bits. For applications requiring better temperature stability, the 4727-01 is available with a guaranteed ± 30ppm of FS/°C drift. As a current to frequency device, the 4727 resolves currents as low as 250pA, allowing operation with full scale input voltages from less than 250mV to greater than 100V. Applications include precision pulse generators, digital integrators and data transmission over a wide common mode voltage range.



Applications Information

When used as shown in Figures 1A & 1B, the factory trimmed 4727 operates as specified without additional components. In particular, the output frequency will be less than 3Hz (0.03% full scale) for zero volts in and between 10.05kHz and 10.15kHz for 10 Volts in.

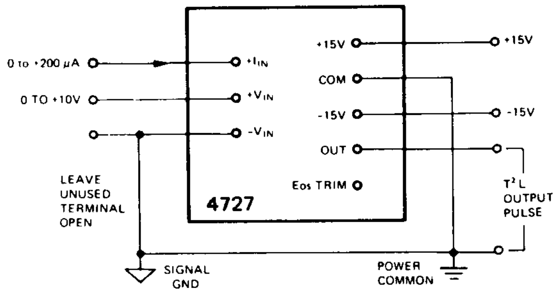


Figure 1A. Positive Input Signals

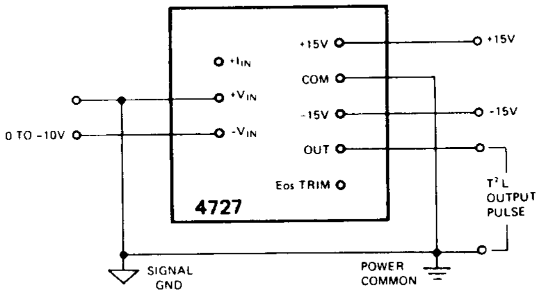


Figure 1B. Negative Input Signals

FEATURES

- ± 0.005%FS Max Nonlinearity
- Low Full Scale and Zero Offset Voltage Drift
- 120dB Dynamic Range
- 80dB CMRR
- − 25°C to + 85°C Guaranteed Operation

APPLICATIONS

- No Drift Integrate/Hold
- High Common Mode Voltage Isolation
- 2 Wire Digital Transmission
- Analog to Digital Converters

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SPECIFICATIONS @ +25°C, $\pm V_{CC}$, ±15 V (unless otherwise indicated)

	TYPICAL		GUARANTEED	
FULL SCALE (FS)				
Ideal Transfer Function	---		$f_{out} = \frac{(V_{in})(10\ kHz)}{10\ V} = \frac{(I_{in})(10\ kHz)}{(+200\ \mu A)}$	
Full Scale Factor (Input for 10 kHz Out)				
$+V_{in}$, $-V_{in}$ (factory trimmed)	---		9.9 V ±0.5% trimmable to 10.00 V	
$+I_{in}$	---		200 μA ±25%	
Range (for specified nonlinearity) ①				
$+V_{in}$ Terminal	+10 μV to +13 V		+100 μV to +11 V	
$-V_{in}$ Terminal	−10 μV to [$-V_{CC}$ +4.9 V]		−100 μV to [$-V_{CC}$ + 4.9 V]	
$+I_{in}$ Terminal	---		+2 nA to 200 μA (±25%)	
Differential [($+V_{in}$) −($-V_{in}$) ③	±12 V		±11 V, (±V_{CC} fault)	
Over Range Max., $+V_{in}$, ($-V_{in}$ = 0)	$+V_{in}$ = 13 V, f_{out} = 13 kHz		$+V_{in}$ = +12 V, f_{out} = 12 kHz	
Dynamic Range	120 dB		100 dB	
Common Mode Voltage ②	+11 V, −10.5 V		±10 V	
CMRR, CMV = ±10 V	80 dB		60 dB for 100 Hz ≤ f_{out} ≤ 10 kHz	
NONLINEARITY ± % FS				
$+V_{in}$ (+100 μV to +11.0 V)	.001		.005	
$-V_{in}$ (−100 μV to $-V_{CC}$ +4.9 V)	.01		.02	
$+I_{in}$ (2 nA to 220 μA)	.001		.005	
$+V_{in}$ (+100 μV to +11.0 V) ⑤	.003		.02	
$-V_{in}$ (−100 μV to $-V_{CC}$ +4.9 V) ⑤	.01		.02	
$+V_{in}$ (+100 μV to +12 V) ⑤	.006		.02	
INPUT				
Zero Offset Voltage, Initial Untrimmed	±1 mV		±3 mV (trimmable to zero)	
Impedance @ $+V_{in}$	---		50 KΩ ±25%	
Impedance @ $-V_{in}$	100 Meg Ω		10 Meg Ω	
Impedance @ $+I_{in}$ (op amp summing point)	Virtual Ground		<0.1 Ω	
STABILITY OF FULL SCALE FACTOR	**4727**	**4727-01**	**4727**	**4727-01**
Temperature Coefficient ($+V_{in}$, $-V_{in}$) ±PPM/°C ④	30	15	50	30
Temperature Coefficient ($+I_{in}$) PPM/°C ④	20	20	---	---
Power Supply Sensitivity ±PPM/% Δ V_{CC} ③	5	5	35	35
Drift: Per Day/Per Month ± PPM	10/30	10/30	---	---
Warm Up Time to .01%/.002% of FS	1 s/100 s	1 s/100 s	---	---
STABILITY OF ZERO OFFSET VOLTAGE				
Temperature Coefficient ④	±6 μV/°C		±20 μV/°C	
Power Supply Sensitivity ± μV/% Δ V_{CC} ③	3		20	
Drift: Per Day/Per Month	20 μV/60 μV		---	
RESPONSE				
Settling Time to .01% for FS step input	---		1 to 2 pulses of new frequency +5 μsec	
Overload Recovery (V_{in} = +20 to V_{in} = +10) or (I_{in} = 500 μA to I_{in} = 200 μA)	0.14 msec		0.25 msec	
OUTPUT WAVEFORM			TTL compatible	
High (positive logic "1")	---		+2.4 V to +5 V (up to 1 TTL Load)	
Low (positive logic "0")	---		≤ 0.4 V @ −16 mA Sink Current	
Pulse Width	---		25 μsec to 50 μsec	
Rise Time/Fall Time (C_{load} ≤ 2000 pF)	2.5 μsec/0.5 μsec		---	
Source Impedance (High)	---		3.5 KΩ ±20%	
POWER REQUIREMENT				
Voltage Range (± V_{CC})	±11.5 V to ±18 V		±12 V to ±18 V	
Voltage Asymmetry (Δ between |$+V_{CC}$|&|$-V_{CC}$|	---		±2 V	
Current (± I_{CC}) @ V_{CC} = ±15 V	±20 mA		±35 mA	
ENVIRONMENT/RELIABILITY				
Operating Temperature	---		−25°C to +85°C	
Storage Temperature Absolute Max.	---		−55°C to +125°C	

Input Protection: All inputs may be shorted to $\pm V_{CC}$ indefinitely without damage.
Output Protection: May be shorted to ground indefinitely; to $+V_{CC}$ for 5 seconds; and to $-V_{CC}$ @ 200 mA indefinitely (crowbar protected, see text).

NOTES

① After trim @ 10 Hz and 10 kHz
② See Figure 5G for definition
③ Constant voltage at Zero trim pin
④ Temperature coefficients measured from −25°C to +85°C
⑤ Measurement, made for ± V_{CC} = ±12 V to ±18 V

Zero & Full Scale Trim

When greater accuracy is required, input offset voltage (E_{OS}) is trimmed to ZERO and Full Scale (FS) output frequency f_{out} is trimmed to 10.00 kHz with external potentiometers as illustrated in Figure 2. (Note: Full Scale trim components should have temperature coefficients similar to Full Scale TC of 4727 being used).

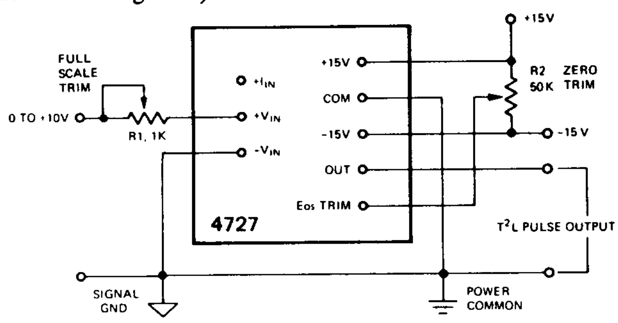


Figure 2A. Positive Voltage Input

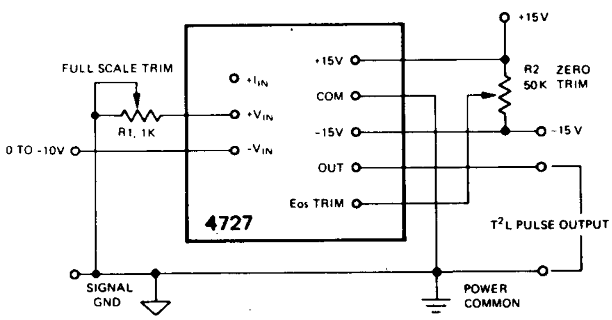


Figure 2B. Negative Voltage Input

TRIM PROCEDURE

1. Apply 10 mV between the + or – voltage input terminal and ground; then adjust R2 for f_{out} = 10 Hz.
2. Apply +10 V between the + voltage input terminal (+V_{in}) and ground or –10 V between the – voltage input terminal (–V_{in}) and ground. Adjust R1 for f_{out} = 10 kHz.
3. Repeat (1) and (2) for precise Zero and Full Scale set. Note: "Zero" is set at 10 Hz out for 10 mV in, because it is very difficult to measure zero Hz out for zero volts in.

Full Scale accuracy for the + current input is ±25%. Greater accuracy is obtained by using the Full Scale and Zero trim circuits shown in Figure 3.

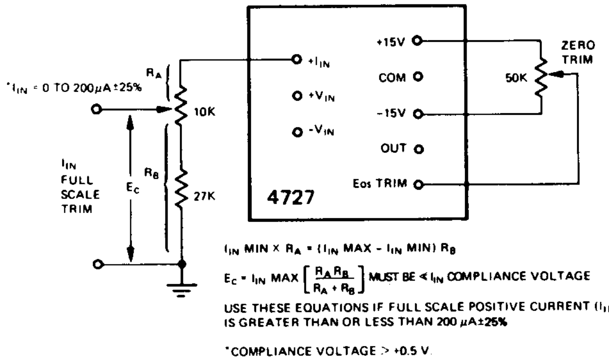


Figure 3. Zero & Full Scale Trim for Positive Input Currents

THEORY of OPERATION

To take maximum advantage of the 4727's versatility (Figure 4), a functional block diagram and theory of operation is provided. With this information, input and output circuitry are easily modified to handle virtually any signal or load.

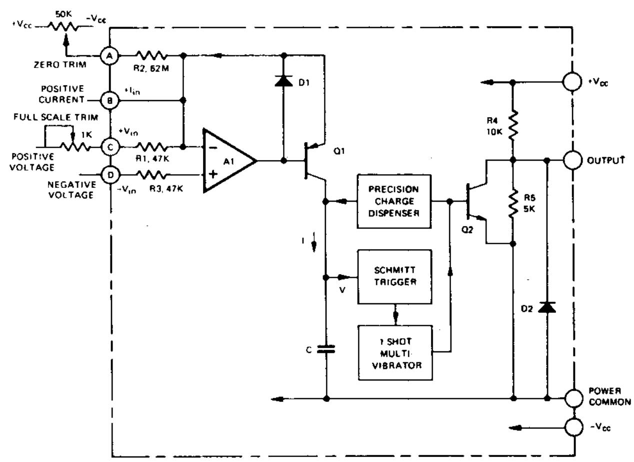


Figure 4. Model 4727 Simplified Block Diagram

The 4727 V-to-F is a free running (astable) voltage controlled multivibrator (See Figure 4). The effective currents from the three inputs (A, B, and C) are summed at the minus input of op amp A1. A1 and transistor Q1 form a precision current pump, producing current I from the collector of Q1, which is a linear function of the A1 input currents. Current I charges capacitor C at a rate which is a precise linear function of the 4727's input signal.

When the voltage impressed on C (due to I) reaches a fixed precision threshold, the Schmitt-Trigger output changes state and triggers the one-shot (monostable) multivibrator, which in turn produces a constant width output pulse. This pulse performs two functions. Amplified by Q2, it is the output of the 4727 and functionally activates the Precision Charge Dispenser (PCD). The PCD discharges C to the same "zero" level every time an output pulse is produced. Thus, capacitor C is repeatedly charged between two precise voltages at a rate which is a linear function of the 4727 input signal, producing the waveforms shown in the timing diagram, Figure 7. That is, the rate of charging C, (the repetition rate of charging C and thus the output frequency) are functions of the 4727 voltage and/or current inputs.

TRIM THEORY

The 4727 input circuit Zero and Full Scale trim techniques are based on the input circuit amp (A1, Figure 4) and the user may treat the input as such within certain limits. No combination of signals may be applied to the 4727 inputs which will drive the A1 output positive. That is, a frequency output will not result if the total current into the 4727 positive inputs (A1, summing point) becomes negative with respect to the 4727 negative input. If this occurs, D1 will become forward biased, Q1 cut off, I becomes zero, and f_{out} becomes zero. The inherent current Full Scale Factor is 200μA, ±25% to give 10 kHz out. All current trimming must take this ±25% tolerance into account. Factory trims the full scale ±V_{in} to within ±0.5%.

FULL SCALE FACTOR CHANGE

The specified Full Scale Factor for the 4727 is 9.9 V ±0.5% (or + 200μA, ±25%) to produce 10.00 kHz out. Many applications require 10 kHz for other (larger or smaller) Full Scale input signals and polarities. Figures 5A through 5F illustrate how to operate the 4727 with such signal levels.

Magnitude of V_{IN} > 10 Volts

The 4727 can be operated with input voltages greater than +10 by connecting a fixed resistor and trim potentiometer in series with the + voltage input (see Figure 5A). For voltages more negative than −10 V, the attenuator network of Figure 5B performs well. Zero Trim and other adjustments remain the same as in Figure 2.

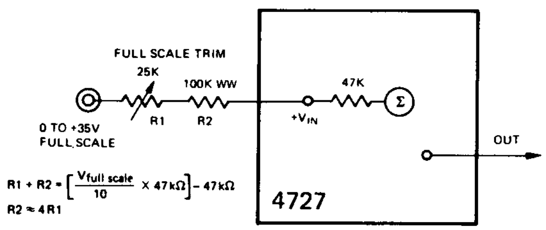


Figure 5A. Full Scale +Vin Greater Than +10V

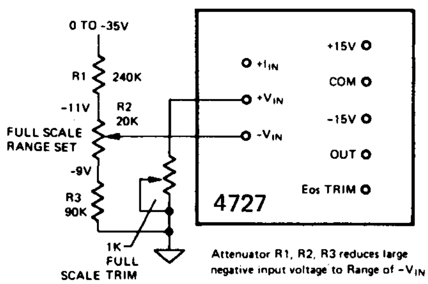


Figure 5B. Full Scale Input Voltage More Negative than −10V

−10 Volts < Full Scale V_{IN} < +10 Volts

If the full scale input voltage is between +10 μV and +1 V, (100 dB) the full scale output is set at 10 kHz by using the + current input terminal with a series resistor as shown in Figure 5C.

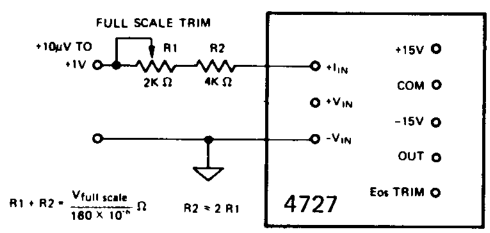


Figure 5C. Full Scale Input Between ≈+10μV and +1V

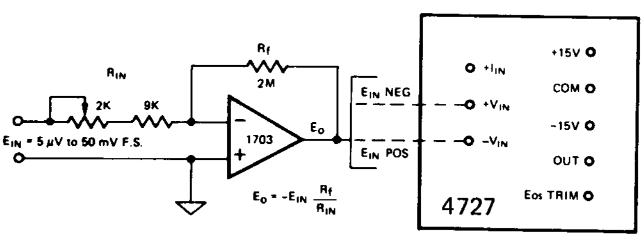


Figure 5D. Full Scale Input Voltage Between −.1 V and +.1V

When the Full Scale Input Signal is between −0.1 volts and +0.1 volts, a low drift amplifier such as the TP 1703 should be used to raise the signal to 10 V. See Figure 5D.

Reduce Full Scale f_{out} Below 10 kHz

In some applications, a Full Scale output frequency of less than 10 kHz is required when the input signal is 10 volts or greater. The circuits of Figures 5 and 6 which show attenuation of the input signal to 10 volts are used to decrease the Full Scale input signal below 10 V and, therefore, Full Scale f_{out} below 10 kHz.

To maximize use of the 4727's dynamic range, however, the input signal is conditioned to + or −10 V Full Scale and a binary or BCD frequency divider (counter) is connected to the output. Any TTL, CMOS, or HNIL device may be used, from a simple divide by 10 unit such as the TTL 54/74 90A to a programmable divider such as the CMOS CD4054, which can divide by any number from 3 to 15,999.

If the 4727 FS output is set at 10 kHz, as shown in Figure 5E, counter output will be 1 kHz (minimum output frequency will be 1 milliHertz).

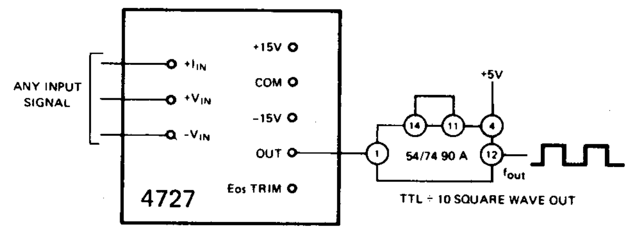


Figure 5E. Full Scale Output Less Than 10kHz When Vin Is Equal To Or Greater Than 10V

Full Scale Input Current Greater Than +200 μA

If the full scale input current is greater than +200μA, the "current splitter" circuit of Figure 3 is used. As noted in Figure 3, the voltage developed at the wiper of the potentiometer must be less than the compliance voltage of the current source. A negative input current can be conditioned by passing it through a resistor connected between $-V_{in}$ and signal common and thus producing a negative voltage. (Trim per Figure 2B at $+V_{in}$). The compliance voltage of the current source, however, must be greater than the maximum voltage developed across the resistor.

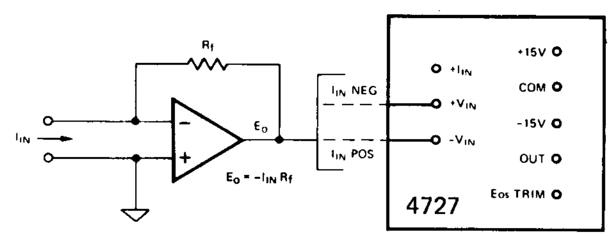


Figure 5F. Full Scale Input Currents Negative, Or Less Than 200μA

The best way to CONDITION CURRENT SIGNALS is with the classic current to voltage converter circuit shown in Figure 5F. With this circuit and the "right" amplifier, virtually any current (even femtoamps) will provide a positive or negative 10 V full scale input to the 4727 with no compliance voltage problem.

Differential Inputs

The 4727 $+V_{in}$ and $-V_{in}$ terminals represent a true differential input capable of accepting a signal from a balanced line, a thermistor bridge or a signal source sitting at a common mode voltage. The 4727's differential input eliminates the need for a differential amplifier.

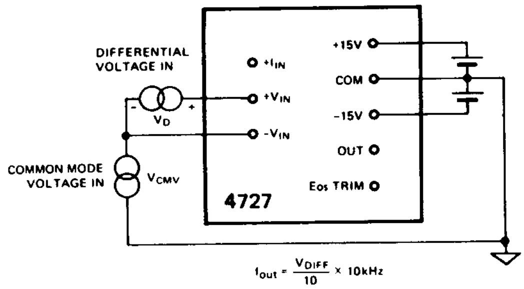


Figure 5G. Definition of Differential & Common Mode Voltage

To use the 4727 voltage inputs differentially, several simple conventions (definitions) must be observed as illustrated in Figure 5G.

1. Common Mode Voltage (CMV) is defined as the voltage between ±Vcc common and the negative V_{in} pin.
2. The positive V_{in} pin must always be positive with respect to the negative V_{in} pin.
3. CMV Range is typically between $+V_{CC}$ -4V and $-V_{CC}$ +5V.
4. The differential (floating, balanced) signal source must be returned to $\pm V_{CC}$ common and must not create voltages which exceed the limits set by 1, 2, and 3.
5. $f_{out} = \frac{(+V_{in}) - (-V_{in}) \text{ X } 10 \text{ kHz}}{10 \text{ V}}$.

BIPOLAR SIGNALS – SCALE EXPANSION – FAST SIGNALS

Operate With Bipolar Input Signals

The 4727 can not operate with bipolar (e.g., -5 V to +5 V) input signals when connected as shown in Figures 1 and 2. To handle such inputs, it is necessary to offset the zero. That is, produce a pulse train out for "zero" volts in. For example: If the $+V_{in}$ pin is connected to zero volts and the $-V_{in}$ pin is connected to a fixed -5 volts, the output of the V-to-F has been "offset" to 5 kHz. If the $+V_{in}$ pin is now connected to -5 V, f_{out} is 0 kHz; if $+V_{in}$ is +5 V, f_{out} is 10 kHz. The offsetting may be performed at the $+V_{in}$ pin and the signal applied to the $-V_{in}$ pin or the $+I_{in}$ pin; or the $+I_{in}$ pin may be used for the fixed offset. Offsetting may combined with all of the techniques of Figures 5 and 6 to provide versatile signal conditioning.

Expand a Portion of Scale to Full Scale

An input signal is often a small voltage change impressed on a larger fixed voltage. This situation is handled by nulling (offsetting) the D.C. or unchanging component of the input signal at one input and adjusting the Full Scale Gain Factor at another so the variable portion of the input signal causes the output frequency to cover the full excursion from 0 Hz to 10 kHz. Such a signal is a voltage level which varies between +4 and +6 volts. To implement offsetting, connect $+V_{in}$ to -4 V. Since the actual signal is 2 V (6 V -4 V), connect it to $+I_{in}$ in series with resistor and trim pot to generate 200 μA with 2 V.

When the input varies between +5 V and +15 V (signal = 10 V), implement offsetting by connecting $-V_{in}$ to +5 V and apply signal to $+V_{in}$. Trim per Figure 4. If the input varies between +30 V and +50 V (signal = 20 V), implement offsetting by connecting -30 V to + I_{in} through a 150 kΩ resistor and series pot. Connect the signal to $+V_{in}$ through a 100 kΩ resistor and series pot. Ground the $-V_{in}$ input.

Operate With Fast Signals

A basic V-to-F application requires operation with rapidly changing input signals. For example, the output of a load cell may change from 0 to Full Scale (or Full Scale to 0) in one millisecond. To accurately handle this signal, the output of the V-to-F must be able to change faster than the input.

The basic response or settling time of the 4727 for any step input is one period of the new frequency plus 5μsec. That is, if the input is changed one volt from 1.001 volts to 0.001 volts, the new frequency is one Hertz and response time is one second +5μsec. When the input changes from 11 volts to 10 volts, the new frequency is 10 kHz, one period is 100 μsec, and response time is 105 μsec. Therefore, if the V-to-F input signal changes between 0 and Full Scale in one millisecond, the output frequency of the V-to-F for zero volts in must be offset to a new frequency, the period of which is less than the one millisecond required for the input to change. The Full Scale value of the input signal is then adjusted so the V-to-F will operate between this offset or zero frequency and the maximum Full Scale frequency. In Figure 6 a zero to +1 volt signal is shown providing an output frequency which will vary between 9 kHz and 10 kHz.

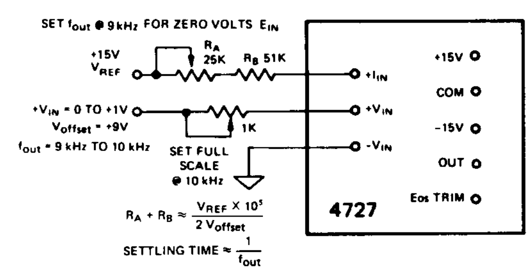


Figure 6. 4727 With Zero Frequency Offset to 9kHz to Decrease Settling Time

HOW TO USE 4727 OUTPUT

The TTL LOGIC pulse train from the 4727 is designed to drive at least one TTL load over the power supply range +12 V to +18 V. At +15 volts, it can drive 10 TTL loads. The output circuit (see Figure 4) is a single transistor Q2 connected as a saturated switch with pull-down resistor R5. When Q1 is on, the output is at "zero" volts. When Q2 is off, the output voltage is $+V_{CC}/3$ or +5 V when $+V_{CC}$ = +15.

Output Protection (+V_{CC}, Common, -V_{CC})

The 4727 output (collector of Q2) may be shorted to ground indefinitely without damage, however, since Q2 is ON most of the time, a short to +V_{CC} will cause certain catastrophic failure in about 5 seconds.

Failure due to a short to -V_{CC} is prevented by the "CROWBAR" diode D2. This diode will conduct 1 amp for 2 minutes, 100 mA indefinitely, and will survive one 25 amp surge such as the discharge of a 500 μF capacitor on the output of the -V_{CC} power source.

Square Wave Output

The output of the 4727 is a train of 37μsec (nominal) pulses (see Figure 7). A symmetrical (square wave) output for driving highly capacitive or noisy transmission lines is obtained with a D or JK flip flop as shown in Figure 8.

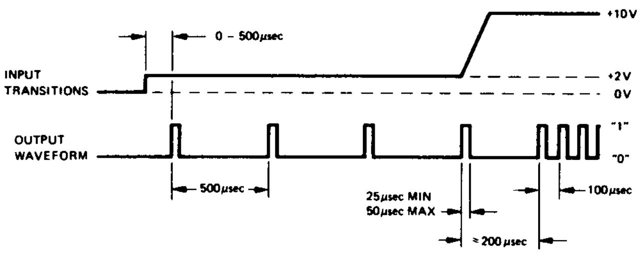


Figure 7. Typical Waveforms, Showing Timing Relationships

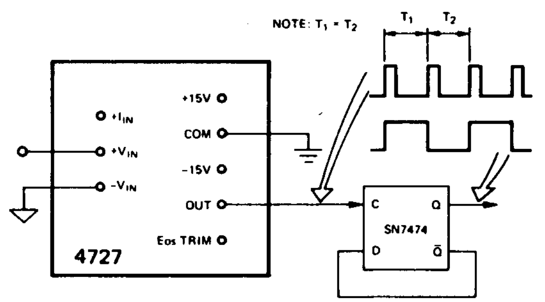


Figure 8. Square Wave Output using D Type Flip Flop

Isolated Output

By supplying the 4727 from floating ±V_{CC} and driving an optical coupler with its output pulses (see Figure 9) analog signals referenced to high common mode voltages (CMV) are transmitted across the CMV. The input - output voltage rating of the power supply and optical coupler are chosen to achieve the required voltage isolation.

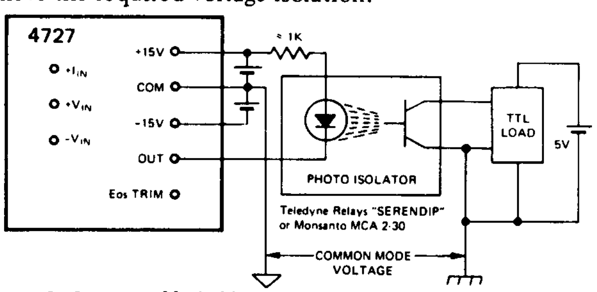
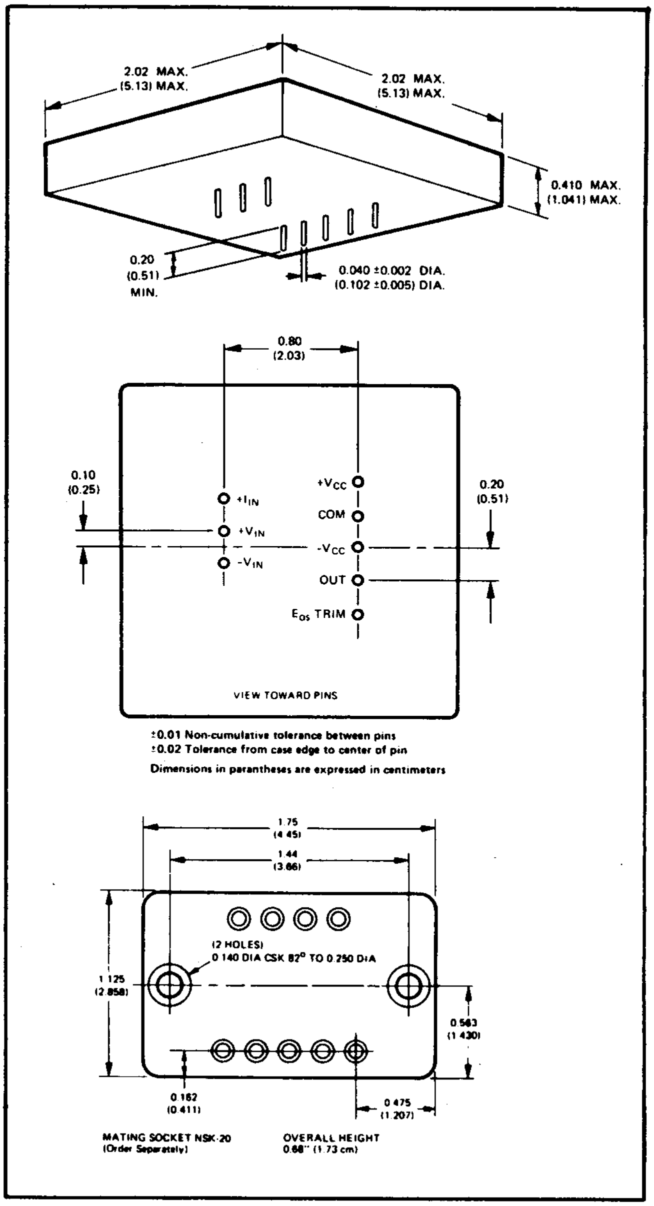
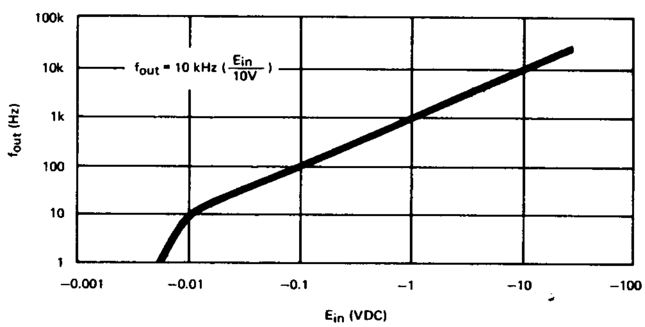


Figure 9. Common Mode Voltage Isolation Using Optical Coupler

CMOS Logic

The 4727 output circuit is easily adapted to drive CMOS. It is only necessary to parallel R4 (Figure 4) with a 680Ω resistor (output to +V_{CC}). The output is then 0.9 (+V_{CC}). This additional pull-up resistor also decreases pulse rise time to drive larger capacitive loads.





Ideal Transfer Function

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