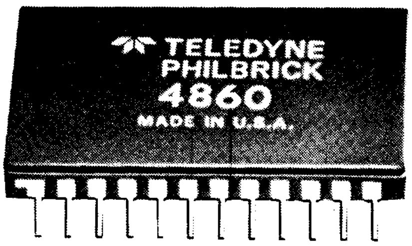
Fastest 12 Bit Sample-Hold Amplifier

4860



The 4860 is the fastest high resolution sample/hold (track/hold) amplifier available. It is the only high speed sample/hold that guarantees acquisition time and sample-to-hold settling time (a S/H's two throughput limiting specifications) to ±0.01% and not to only ±0.1% or ±1%. The 4860 will acquire a full 10V signal to ±0.01%FS (equivalent to ±0.005%FSR or ±1mV) in 200nsec maximum. The unit will then track signal components up to 16MHz. In the track mode, offset error is typically ±0.5mV, and gain error is typically ±0.05%. When commanded to the hold mode (aperture time is 6nsec and aperture jitter is ±50psec), the 4860's output will settle to within ±0.01%FS (±1mV) of its final value in 100nsec maximum. Pedestal is a low ±2.5mV. Once in hold, output droop rate is a low 5μV/μsec maximum. Feedthrough attenuation at 2.5MHz is an impressive 74dB.

A 24 pin dual-in-line package, a gain of −1, an input/output range of ±10V, and TTL compatibility make the 4860 pin compatible with the Analog Devices/Computer Labs HTC-0300. Being a second generation design however, it is superior to that unit in almost every performance specification. Faster switching and better feedthrough attenuation are the result of our unique MOSFET switching scheme. Faster acquisition and settling times and considerably lower droop are the result of our own high speed, FET input op amp designs.

The 4860 is ideally suited for 12 to 14 bit high speed data acquisition/distribution systems. In a ±10V system, its ±0.01%FS (±0.005%FSR) linearity is equivalent to better the ±½LSB for 13 bits. Its low ±50ps aperture uncertainty enables it to accurately sample (to ±½LSB in 12 bits) signals with slew rates up to 24.4V/μsec. Its low 5μV/μsec output droop rate enables it to hold signals to ±½LSB in 14 bits for up to 125μsec. The 4860 is functionally laser trimmed at the factory for offset, pedestal and gain errors, and it is designed to be used without external adjustments. If system requirements call for tighter accuracies, units can be selected at the factory or adjustments can probably be made at the A/D or D/A used with the 4860.

For military/aerospace applications, the 4860 is available for fully specified operation from −55°C to +125°C with high reliability screening to MIL-STD-883, Method 5008 (add -83 to selected part number).

FEATURES

- 200nsec Max Acquisition Time 10V Step to ±0.01%FS
- 100nsec Max Sample-to-Hold Settling Time
- ±50psec Aperture Jitter
- 74dB Feedthrough Attenuation
- TTL Compatible
- HTC-0300 Pin Compatible

APPLICATIONS

- Transient Recorders
- Fast Fourier Analysis
- High Speed DAS's
- High Speed DDS's
- Analog Delay and Storage

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ABSOLUTE MAXIMUM RATINGS

± 15V Supply Voltage (± V_{CC}, Pins 24, 22)	± 18 Volts
+ 5V Supply Voltage (+ V_{dd}, Pin 9)	− 0.5 to + 7 Volts
Analog Input (Pin 13) (Note 1)	± 18 Volts
Digital Input (Pins 11, 12)	− 0.5 to + 5.5 Volts
Output Current (Note 2)	± 65 mA
Operating Temperature Range	− 55°C to + 125°C
Specified Temperature Range	
4860	0°C to + 70°C
4860-83 (Note 3)	− 55°C to + 125°C
Storage Temperature Range	− 65°C to + 150°C

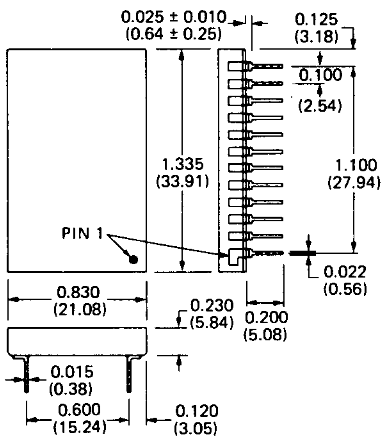
SPECIFICATIONS (T_A + 25°C, V_{CC} = ± 15V, and + 5V, unless otherwise indicated).

PARAMETER	MIN.	TYP.	MAX.	UNITS
ANALOG INPUT/OUTPUT				
Input/Output Voltage Range	± 10.25	± 11.5		Volts
Input Impedance		1		kΩ
Output Current (Note 2)			± 40	mA
Output Impedance		0.1		Ω
Maximum Capacitive Load		250		pF
DIGITAL INPUT				
Logic Levels (Note 4): Logic "1"	+ 2.0		+ 5.0	Volts
Logic "0"	0		+ 0.8	Volts
Loading (Note 5)		1		TTL Load
TRANSFER CHARACTERISTICS				
Gain		− 1.00		V/V
Gain Accuracy		± 0.05	± 0.1	%
Gain Linearity Error (Note 6)		± 0.005	± 0.01	%FS
Offset Voltage (Sample Mode)		± 0.5	± 5	mV
Pedestal (Note 7)		± 2.5	± 20	mV
Stability: Gain Drift		± 0.5	± 5	ppm/°C
Offset Drift (Sample Mode)		± 3	± 15	ppm of FSR/°C
Pedestal Drift		± 4		ppm of FSR/°C
DYNAMIC CHARACTERISTICS				
Acquisition Time (Notes 6, 8):				
10V step to ± 0.01%FS (± 1mV)		160	200	nsec
10V step to ± 0.1%FS (± 10mV)		100	170	nsec
10V Step to ± 1%FS (± 100mV)		90		nsec
1V Step to ± 1%FS (± 100mV)		75		nsec
Settling Time, Sample to Hold (Note 9)				
to ± 0.01%FS (± 1mV)		60	100	nsec
to ± 0.1%FS (± 10mV)		40		nsec
Sample to Hold Transient		180		mVp-p
Aperture Delay Time		6		nsec
Aperture Jitter		± 50		psec
Output Slew Rate		300		V/μsec
Small Signal Bandwidth (− 3dB)		16		MHz
Droop: + 25°C		± 0.5	± 5	μV/μsec
+ 70°C		± 15		μV/μsec
+ 125°C (4860-83)		± 1.2		mV/μsec
Feedthrough (2.5MHz, 20Vp-p input)		74		dB
POWER SUPPLIES				
Voltage Range: ± 15V Supplies		± 3		%
+ 5V Supply		± 5		%
Power Supply Rejection Ratio		± 0.5		mV/V
Quiescent Current Drain: + 15V Supply		+ 21	+ 25	mA
− 15V Supply		− 22	− 25	mA
+ 5V Supply		+ 17	+ 25	mA
Power Consumption		730	875	mW

SPECIFICATION NOTES

1. Analog input signal should not exceed supply voltage.
2. The 4860's output is current limited at approximately ± 65mA, and the unit can withstand a sustained short to ground. Shorts to either supply will result in destruction. For normal operation, load current should not exceed ± 40mA.
3. The 4860-83 is specified for − 55°C to + 125°C operation and is processed and screened to the requirements of MIL-STD-883, Method 5008.
4. See Applications Information for use of Hold and $\overline{\text{Hold}}$ inputs.
5. One TTL load is defined as sinking 40μA with a logic "1" applied and sourcing 1.6mA with a logic "0" applied.
6. FS stands for Full Scale and is equivalent to 10 volts. FSR stands for Full Scale Range and is equivalent to 20 volts. For a 12 bit system, 1 LSB = 0.024%FSR.
7. Pedestal refers to the unwanted step in output voltage that occurs as a S/H is switched from the sample to hold mode. For many S/H's, pedestal amplitude is a function of input/output voltage level. For the 4860, pedestal is constant regardless of input/output level.
8. Acquisition time is tested with no load and is relatively unaffected by capacitive loads to 50pF and resistive loads to 250Ω.
9. Sample to hold settling time refers to the time interval between the point at which a device is commanded from the sample to the hold mode and the point at which the analog output (following a transient) settles to within a specified error band around its final value.

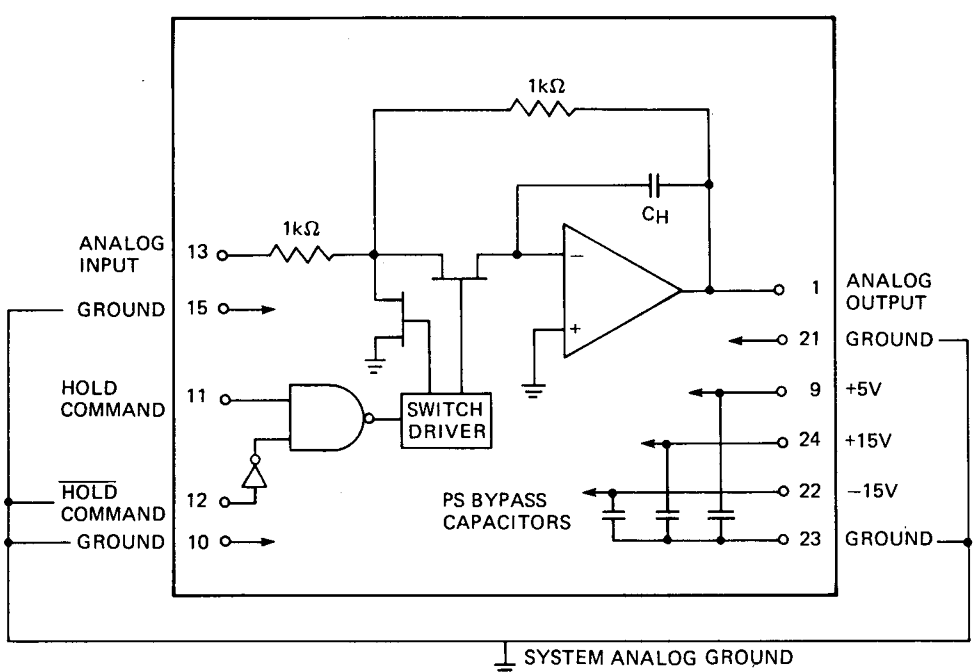
Package Dimensions 24 Pin DIP



Pin Designations

1	Analog Output	24	+15V Supply
2	N/C	23	Ground
3	N/C	22	−15V Supply
4	N/C	21	Ground
5	N/C	20	N/C
6	N/C	19	N/C
7	N/C	18	N/C
8	N/C	17	N/C
9	+5V Supply	16	N/C
10	Ground	15	Ground
11	Hold Command	14	N/C
12	$\overline{\text{Hold}}$ Command	13	Analog Input

Functional Block Diagram



Applications Information

Grounding and Bypassing

With proper grounding and bypassing, the 4860 will meet all its published performance specifications without any additional external components. The device has four ground pins (pins 10, 15, 21 and 23), and all must be tied together and connected to system analog ground as close to the package as possible. It is preferable to have a large analog ground plane beneath the 4860 and have all four ground pins soldered directly to it. Pin 10 is particularly ground noise sensitive because in the actual construction of the 4860, most of the digital elements that constitute the switch drive circuit are grounded to pin 10. Noise in the switch drive circuit couples directly through to the main op amp summing junction—the most noise sensitive point in any S/H circuit. Therefore, most digital ground currents will enter or leave the 4860 through pin 10, and in order to keep the output clean, care must be taken to ensure that no ground potentials can exist between pin 10 and the other ground pins. This is why pin 10 must be tied to the analog and not the digital ground system. For the same reason, the +5V digital logic supply (pin 9) should be kept as clean as possible. This supply, as well as the ±15V supplies (pins 24 and 22), is bypassed to ground with 0.01μF ceramic capacitors inside the 4860's package. In critical applications, additional external 0.1μF to 1μF tantalum bypass capacitors may be required.

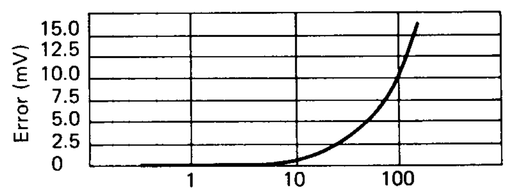
Sample-Hold Command

A TTL logic "0" applied to pin 11 (or a logic "1" applied to pin 12) will put the 4860 into the sample (track) mode. In this mode, the device acts as an inverting unity gain amplifier, and its output will follow (track) its input. A logic "1" applied to pin 11 (or a logic "0" applied to pin 12) will put the 4860 into the hold mode, and the output will be held constant at the level present when the hold command was given. If pin 11 is used to control the 4860, pin 12 must be connected to digital ground. If pin 12 is used to control the 4860, pin 11 must be tied to +5V. Pins 11 and 12 each present 1 TTL load to the digital drive circuit.

Capacitive and Resistive Loading

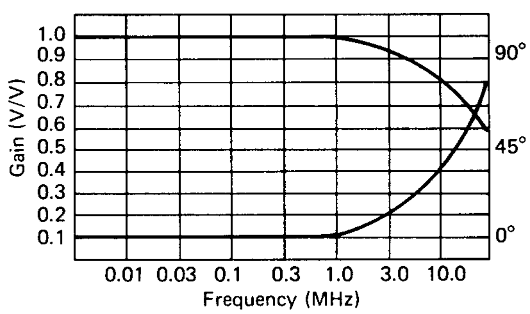
To avoid possible oscillations, current limiting, and performance variations over temperature, the 4860's output loading has certain restrictions. The maximum capacitive load to avoid oscillation is typically 250pF. Recommended resistive loading is 500Ω, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω and capacitive loads up to 50pF. Higher capacitances will affect both acquisition and settling time.

Accuracy Error Due to Aperture Uncertainty

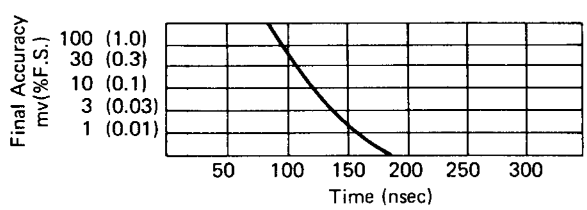


Input Signal Slew Rate (V/μsec)
Aperture Jitter Window = 100psec
For v(t) = 10sinωt, dv/dt (max) = 20πf

Track Mode Gain Amplitude and Phase Response



Acquisition Accuracy vs. Acquisition Time for a 10V Step



Aperture Jitter

The most common use of sample(track)-hold amplifiers is ahead of A/D converters to permit the accurate digitizing of signals with slew rates (frequencies) much higher than the A/D's alone can handle. The standard rule of thumb for obtaining desired accuracy in successive approximation type A/D conversion is to ensure that the analog input signal does not change by more than ± ½LSB during the conversion time. Applying this rule to a given A/D converter, one can calculate an input slew rate limit beyond which accurate digitizing is impossible. The slew rate limit can then be converted to a frequency limit if one chooses to speak in those terms. Example: the Teledyne Philbrick 4189 is a 12 bit 5μsec A/D converter. If it is operated on its ±10V input range, 1LSB (0.024%FSR) is equivalent to 4.88mV, and ½LSB is equivalent to 2.44mV. If the input is not allowed to change more than 2.44mV in 5μsec, the 4189's input slew rate limit is ±0.488mV/μsec. If one were trying to accurately digitize a ±10V sine wave ($v(t) = 10\sin\omega t$), its frequency would have to be below 7.8Hz, i.e., $dv/dt\ (max) = 10\omega\cos\omega t(max) = 10\omega = 20\pi f$ must be less than 0.488mV/μsec, and therefore, f must be less than 7.8Hz.

A sample-hold in front of an A/D converter can "freeze" the converter's input signal whenever it is necessary to make a conversion. Though the presence of the S/H reduces system throughput (the S/H acquisition time has to be added to the A/D conversion time to determine how often one can obtain fresh digital data), it permits the accurate digitizing of input signals with much higher slew rates (frequencies). How is this accomplished? Once a S/H (T/H) has acquired an input signal and is tracking it, the S/H can be commanded to hold at any instant. There is normally a small delay between the time the unit is commanded to hold and the time it actually holds. This delay is called aperture delay time or aperture time delay, and it normally does not present a problem as the hold command signal can simply be advanced in time to make the amplifier hold when one wants it to hold. Aperture delay time is not always exactly the same, however, as a given device takes sample after sample. The sample to sample variation in aperture delay time is called aperture jitter, and though aperture delay time is not really a problem, aperture jitter is. This is because it is impossible to control or compensate for aperture jitter. Since we have no control during the small period of aperture jitter, we would like our input signal to change as little as possible during this period. To return to our rule of thumb, we don't want the input to change by more than ± ½LSB. Therefore, if we're using a S/H in front of an A/D converter, the slew rate limitation is no longer ± ½LSB during the conversion time but ± ½LSB during the aperture jitter time. The 4860 has a ±50psec aperture jitter. That means there is a 100psec period during which an input signal should not change more than ± ½LSB. If you're using a 4860 in front of a 4189 operating on its ±10V range (½LSB = 2.44mV), the input signal slew rate limitation for accurate digitizing is 2.44mV/100psec = 24.4V/μsec. This is equivalent to the highest slew rate one would encounter in a ±10V sine wave with a frequency of 388kHz—a considerable improvement over the 7.8Hz sine wave the 4189 could accurately digitize without a S/H. Needless to say 388kHz to 7.8Hz has the same ratio as 5μsec (the 4189's conversion time) to 100psec (the 4860's aperture jitter).

Loose ends—this procedure for determining how fast a signal a given S/H permits one to digitize assumes the output droop rate of the chosen sample-hold is low enough to keep the A/D's input constant to within ± ½LSB during a conversion time. It also assumes that at the input slew rate (frequency) of interest, the S/H's output is not slew rate (bandwidth) limited. Lastly, the fact that a given S/H-A/D combination can accurately digitize the fastest portions of a 388kHz sine wave does not at all mean that the same combination can be used to digitize that signal for reproduction purposes. If you have to sample a 388kHz sine wave at twice its frequency, you have take a sample every 1.25μsec. The 4860-4189 combination can take a sample only every 5.2μsec because the 4860 has a 200nsec signal acquisition period and the 4189 needs 5μsec to convert.

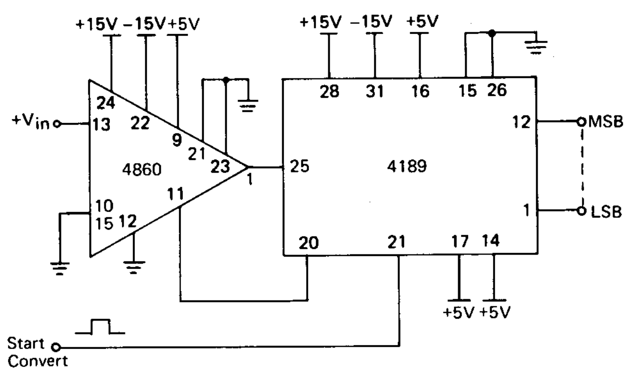
Using the 4860 with A/D Converters

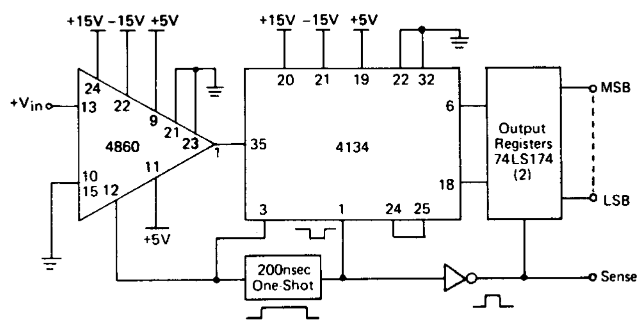
There are two important considerations when using S/H's to drive successive approximation A/D's. The first is a dual requirement—the S/H's output stage should exhibit a very low impedance compared to the A/D's input impedance (usually 1 to 10kΩ) at frequencies up to five times the A/D's clock period, and the S/H should be able to recover from current transients in a time interval smaller than the A/D's clock period. These requirements are based on the fact that as a successive approximation A/D's internal D/A converter changes its output current just prior to the determination of each output bit, the S/H will be required to sink or source large high frequency current transients and recover within one clock period. In the hold mode, the 4860's output impedance is typically 0.1Ω. Its output typically recovers (to ±0.01%) from a 2mA step in less than 100nsec. The second consideration involves the S/H's sample-to-hold transient settling time. If the same timing pulse that puts the S/H into the hold mode intitiates the A/D conversion, the transient settling time has to be short enough to ensure that the A/D has a stable, accurate input when it makes the final decision on whether its MSB output should be a "1" or "0". This decision normally takes place one clock period after a conversion has begun.

In most applications using the 4860 in front of a successive approximation A/D converter, the 4860's S/H command pin can be driven directly (or inverted if necessary) from the converter's status output. The status output changes state when the converter receives a convert command, and this change can drive the S/H from the track to the hold mode. The change in state of the A/D's status output at the end of the conversion can put the S/H back into the track mode. The diagram below illustrates a 4860 mated with a 4189 in this manner. Since the 4189's MSB output is not set to its final value until one clock period (approximately 500nsec) after a conversion begins, the 4860's sample-to-hold transient will be completely settled, and no extra precautions are necessary.

If the A/D is an internal-clock device and it has to make continuous conversions, it may be necessary to use a one-shot to generate the 4860's sample pulse. In the diagram below, the 4860 is mated to a Teledyne Philbrick 4134 (2μsec 12 bit A/D). At the end of each conversion, the falling edge of the 4134's status output fires a 200nsec one-shot as it latches (through an inverter) the output data. The one-shot's output serves as the convert command for the 4134 and the S/H command for the 4860. It's rising edge puts the 4860 into the signal acquisition mode and the 4134 into the reset state. Its falling edge puts the 4860 into the hold mode and initiates a conversion. The sense output will be a 0 when output data is valid and a 1 when output data is changing. The throughput of this system is 430 conversions/sec. Without the one-shot, the 4134's status output would go low for approximately 70nsec between conversions, and this is not enough time for the 4860 to acquire a new analog signal.

See Teledyne Philbrick 4857, 4189, TPADC85/87, and TP5210 data sheets for additional tips on mating S/H's and A/D's.





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