TELEDYNE PHILBRICK

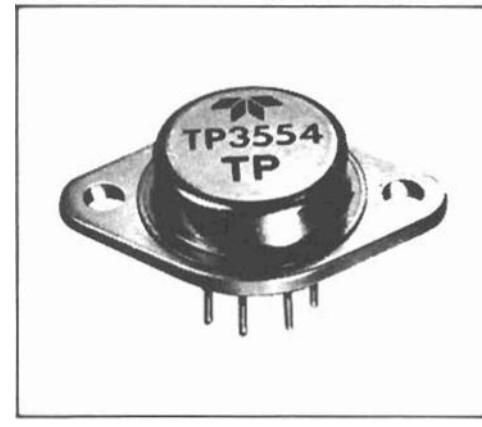
High Speed Wideband Operational Amplifier

TP3554

The TP3554 is a fully differential, wideband operational amplifier with a 2GHz gain-bandwidth product, a 1000V/μsec slew rate, and a full ±10V ±100mA output. Settling time for a 10V step to ±0.01% is guaranteed less than 250nsec, and external compensation allows users to optimize bandwidth, slew rate, or settling time in different applications.

The TP3554 is an improved second source to the Burr-Brown 3554. In most applications, the TP3554 is a drop-in replacement for the BB3554, having similar bandwidth and slew rate characteristics with similar compensation. In other applications, the TP3554's superior design approach will solve many of the problems encountered with the BB3554. The TP3554's improved interior loop stability overcomes the BB3554's pronounced tendency to ring or oscillate at 120MHz, especially at lower gains (higher compensations). The improved loop stability also results in an improved capacitive load capability. The TP3554 has no input overload problems. Input slew rate does not affect settling time, and there are no input rise time restrictions. This eliminates many of the problems encountered in pulse-amplifier applications. The TP3554 has a much lower quiescent current drain (±20mA maximum) and a lower short-circuit output current. For critical low-gain applications, the Teledyne Philbrick 1443 (1000V/μsec guaranteed slew rate at G = 1, 130nsec settling to ±0.01%) is designed for superior stability.

The TP3554 is packaged in a standard TO-3 can. Units are specified for −25°C to +85°C or −55°C to +125°C (-80 and -83 versions) operation. For hi-rel military/aerospace applications, the TP3554-83 is also fully processed and screened to the high reliability requirements of MIL-STD-883, Method 5008.



FEATURES

- Low-Gain Stability
  2GHz Gain-Bandwidth Product
- 1000V/μsec Slew Rate
- ±10V, ±100mA Output
- ±20mA Max Quiescent Current
- −55°C to +125°C Operation
- MIL-STD-883 Screening

APPLICATIONS

- Pulse Amplifiers
- Fast Buffer/Followers
- Fast D/A Converters
- Video Instrumentation
- Video Frequency Filters

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($\pm V_{CC}$, Pins 2, 7)	18 Volts
Input Voltage (Pins 5, 6)	$\pm V_{CC}$
Differential Input Voltage (Pins 5, 6)	± 25 Volts
Output Short Circuit Current (Note 1)	± 150 mA
Operating Temperature Range (Ambient)	– 55°C to + 125°C
Specified Temperature Range (Ambient)	
TP3554	– 25°C to + 85°C
TP3554-80	– 55°C to + 125°C
TP3554-83 (Note 2)	– 55°C to + 125°C
Storage Temperature Range	– 65°C to + 155°C

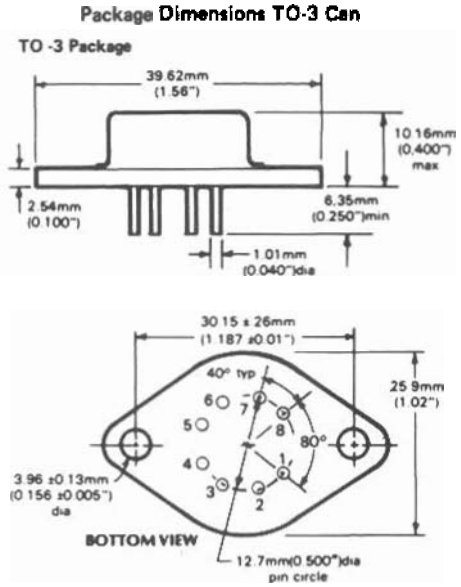
SPECIFICATIONS (T_A = + 25°C, $\pm V_{CC}$ = ± 15V, unless otherwise indicated)

PARAMETER	MIN.	TYP.	MAX.	UNITS
OPEN LOOP VOLTAGE GAIN: R_L = Open	100	106		dB
R_L = 100Ω (Rated Load)	90	96		dB
INPUT CHARACTERISTICS				
Common Mode Voltage for DC Linear Operation		$\pm(V_{CC} - 2)$		Volts
Common Mode Rejection Ratio (Note 3): @ DC	80	86		dB
@ 10MHz		50		dB
DC Input Impedance: Differential		10^{11} // 2		Ω // pF
Common Mode		10^{11} // 2		Ω // pF
Input Offset Voltage:				
Initial (+ 25°C) (Note 4)		± 0.5	± 2	mV
Drift vs. Temperature: TP3554, TP3554-80		± 8	± 15	μV/°C
TP3554-83		± 12	± 25	μV/°C
Drift vs. Supply (PSRR)		± 3	± 100	μV/Volt
Input Bias Current:				
Initial (+ 25°C)		± 10	± 50	pA
Drift vs. Temperature		Doubles every 10°C		
Drift vs. Supply (PSRR)		± 1		pA/Volt
Offset Current: Initial (+ 25°C)		± 2		pA
Drift vs. Temperature		± 1		pA/°C
OUTPUT CHARACTERISTICS				
Output Voltage (I_O = ± 100mA)	± 10.5	± 12		Volts
Output Current (V_O = ± 10V) (Note 1)	± 100	± 125		mA
Output Resistance, Open Loop (f = 10MHz)		20		Ω
Noise (Referred to Input) (Note 5):				
10Hz to 10kHz		2		μVrms
10kHz to 1MHz		2.5		μVrms
Maximum Capacitive Load		75		pF
FREQUENCY RESPONSE				
Gain-Bandwidth Product (Small Signal) (R_L = 100Ω):				
C_{comp} = 0, G = 10	150	225		MHz
C_{comp} = 0, G = 100	425	725		MHz
C_{comp} = 0, G = 1000 (Note 6)	1000	2000		MHz
Unity-Gain Bandwidth: Open Loop, C_{comp} = 0pF		90		MHz
A_{CL} = – 1, C_{comp} = 10pF (Note 7)		35		MHz
Full Power Bandwidth (C_{comp} = 0pF)	16	19		MHz
TIME RESPONSE				
Slew Rate (R_L = 100Ω): C_{comp} = 0pF	1000	1200		V/μsec
C_{comp} = 12pF		+ 330/ – 275		V/μsec
Settling Time: 10V Step to ± 0.01% (± 1mV)		150	250	nsec
10V Step to ± 0.1% (± 10mV)		100		nsec
10V Step to ± 1% (± 100mV)		40		nsec
Overload Recovery Time		1		μsec
POWER REQUIREMENTS				
Nominal Supply Voltages		± 15		Volts
Supply Voltage Range (Derated Performance)	± 5		± 18	Volts
Quiescent Current		± 14	± 20	mA

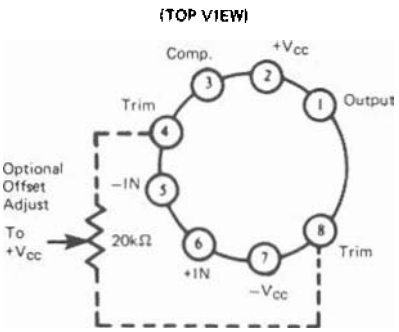
SPECIFICATION NOTES:

1. The TP3554 is short circuit protected to ground with current limiting at approximately ± 150mA.
2. The TP3554-83 is fully screened to the high reliability requirements of MIL-STD-883, Method 5008.
3. ± 10V common mode voltage. See Typical Performance Curves for additional information.
4. Trimmable to zero with 20kΩ optional offset adjust potentiometer betweens pins 4 and 8 with wiper to $+V_{CC}$.
5. Noise is measured with the TP3554 in a very high gain configuration with the input grounded through a small resistance.
6. With R_L = 1kΩ and C_{comp} = 0pF, the typical gain-bandwidth product at G = 1000 is 3GHz.
7. Recommended compensation for inverting gain of 1 configuration is 10pF.

Package Dimensions TO-3 Can



Pin Designations



1. Output
2. $+V_{CC}$
3. Compensation (Pin 3 to 1)
4. Offset Adjust
5. Inverting Input
6. Noninverting Input
7. $-V_{CC}$
8. Offset Adjust

Applications Information

Layout, Grounding and Bypassing

To achieve fully specified performance from the TP3554, certain grounding, wiring, and bypassing precautions are necessary. Grounding is the most important consideration, and a ground plane is a must. The ground plane provides a low resistance, low inductance, common return path for all signals and power returns and also reduces stray signal pickup. It should cover and connect all areas of the pattern side of the printed circuit board that are not otherwise used.

The mechanical circuit layout also is very important. All circuit element leads should be as short as possible. All printed circuit board conductors should be wide to provide low resistance, low inductance connections, and they should be as short as possible. In general, the entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes such as the input terminals of the amplifier. Pin 5, the inverting input, is especially sensitive, and all associated connections must be short. Stray signal coupling from the output to the input or to pin 8 should be minimized. Low resistor values should be used; resistor values less than 5.6kΩ are recommended. This practice will give the best circuit performance, as the time constants formed with the circuit capacitances will have minimal effect on the performance of the amplifier.

Each power supply lead should be bypassed to ground as near to the amplifier pins as possible. A combination of a 0.1μF tantalum capacitor in parallel with a 0.01μF ceramic capacitor is a suitable bypass. In inverting applications, it is recommended that pin 6, the non-inverting input, be grounded rather than being connected to a bias current compensating resistor. This assures a good signal ground at the non-inverting input. A slight offset error will result; however, because the resistor values normally used in high frequency circuits are small and the bias current is small, the offset error will be minimal.

It is recommended that the case of the 3554 not be grounded during use; though it may be if desired. A grounded case will add a slight capacitance to each pin. To an already functional circuit, grounding the case will probably require slight compensation readjustment and the compensation capacitor values will be slightly different from those recommended in the typical performance curves. There is no internal connection to the case.

Optional Offset Adjustment

If the TP3554's guaranteed offset error is too large for a particular application, the initial offset may be adjusted to zero by connecting a 20kΩ linear potentiometer between pins 4 and 8 with the wiper connected to the positive supply. A small, non-inductive potentiometer is recommended. The leads connecting the potentiometer to pins 4 and 8 should be less than 6 inches long to avoid stray capacitance and stray signal pickup. Stray coupling from the output (pin 1) to pin 4 (negative feedback) or to pin 8 (positive feedback) should be avoided.

Compensation

The TP3554 uses external frequency compensation so users can optimize bandwidth, slew rate, or settling time for particular applications. The Bode Plot shows curves for several different compensation capacitors. In addition, several typical circuits show recommended compensation for different applications. The primary compensation capacitor, C_{comp}, is connected between pins 1 and 3. As the performance curves show, higher closed loop gain configurations require less capacitance and an improved gain-bandwidth product will be realized. Note that no compensation capacitor is required for closed loop gains above 55V/V.

The flat high frequency response of the 3554 may be preserved and any high frequency peaking avoided by connecting a small capacitor in parallel with the feedback resistor. This capacitor will compensate for the closed loop high frequency transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. Using small resistor values will keep the break frequency of this zero sufficiently high, avoiding peaking and preserving phase margin. Resistor values less than 5.6kΩ are recommended. The required feedback capacitance value is strongly dependent on circuit layout and closed loop gain. It will typically be 2pF for a clean layout using low resistance (1kΩ) and up to 10pF for circuits using larger resistances.

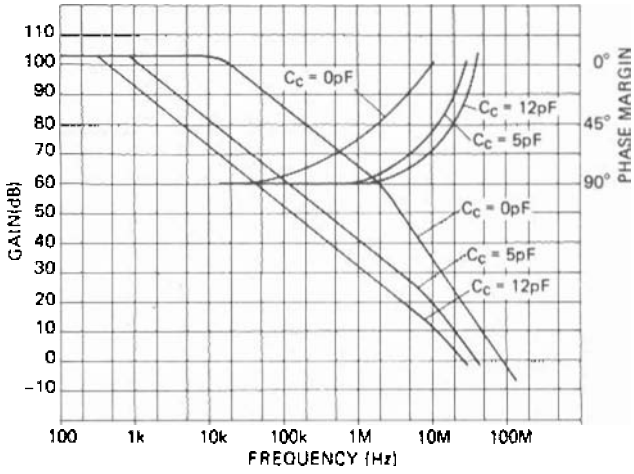
Slew Rate

Slew rate is dependent upon compensation. Decreasing the compensation capacitor value will increase the available slew rate. Stray capacitances may appear to the amplifier as compensation. To avoid limiting the slew rate performance, stray capacitances should be minimized.

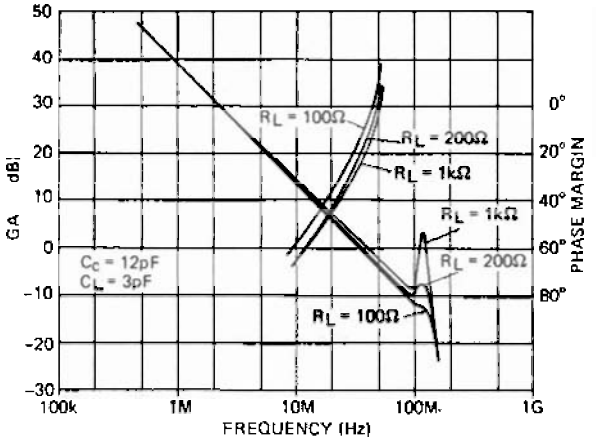
Heatsinking

The 3554 does not require a heatsink for operation in most environments. The use of a heatsink, however, will reduce the internal thermal rise and will result in cooler operating temperatures. At extreme temperature and under full load conditions, a heatsink will be necessary as indicated in the curve. When heatsinking the 3554, it is recommended the heatsink be connected to the amplifier case and the combination not connected to the ground plane. For a single sided printed circuit board, the heatsink may be mounted between the 3554 and the non-conductive side of the PC board, and insulating washers, etc., will not be required. The addition of a heatsink to an already functional circuit will probably require slight compensation readjustment for optimum performance due to the change in stray capacitances. The added stray capacitance from the heatsink to each pin will depend on the thickness and type of heatsink used.

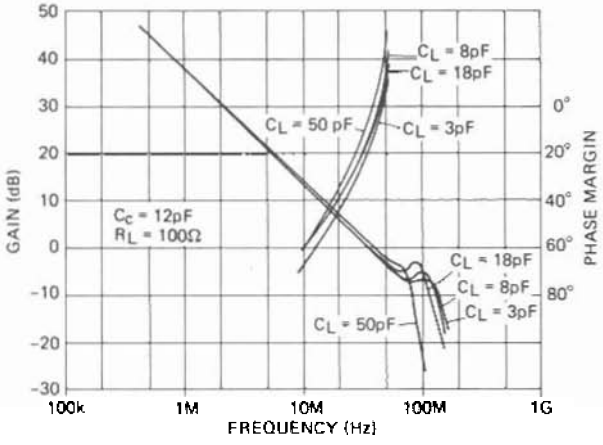
TP3554 Bode Plot



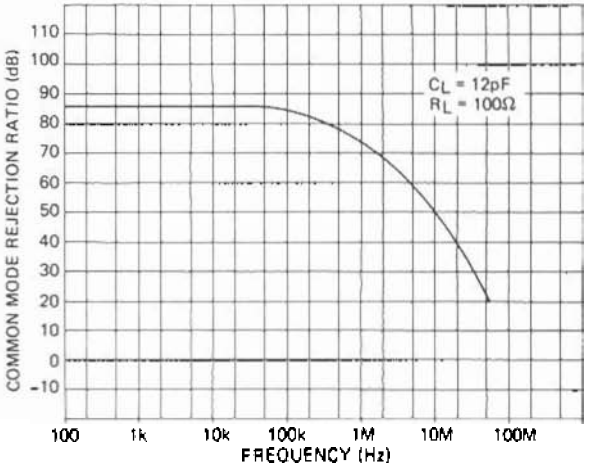
Gain and Phase vs. Frequency for Variable R_L



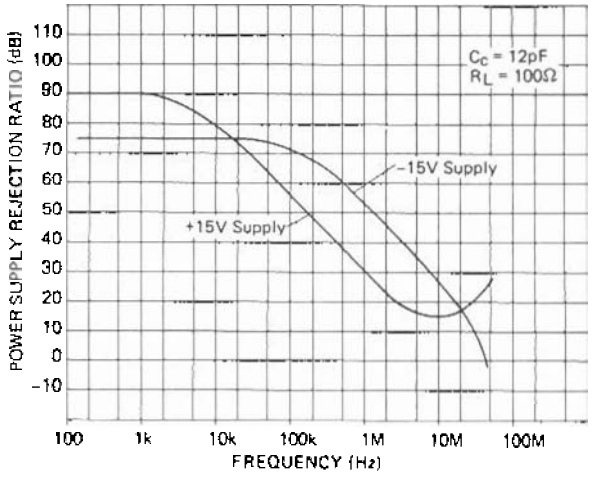
Gain and Phase vs. Frequency for Variable C_L



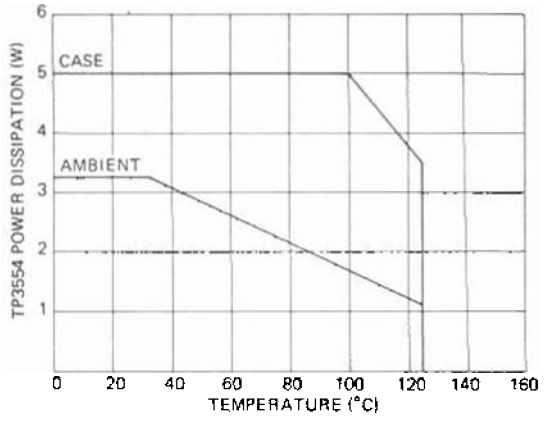
CMRR vs. Frequency



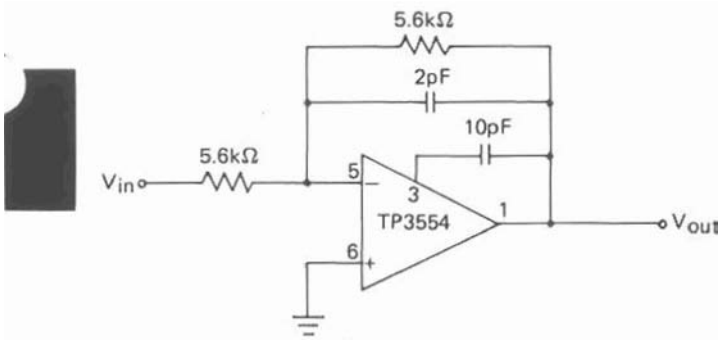
Offset PSRR vs. Frequency



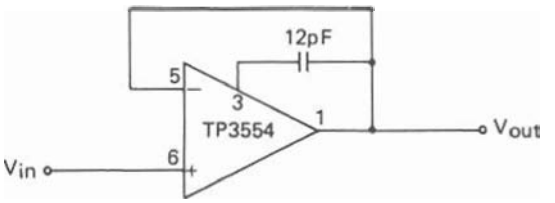
Maximum Power Dissipation



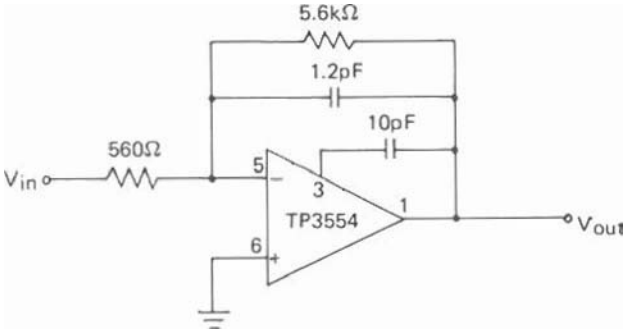
Unity Gain Inverter



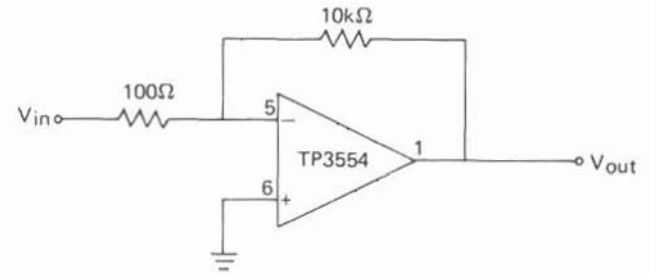
Follower



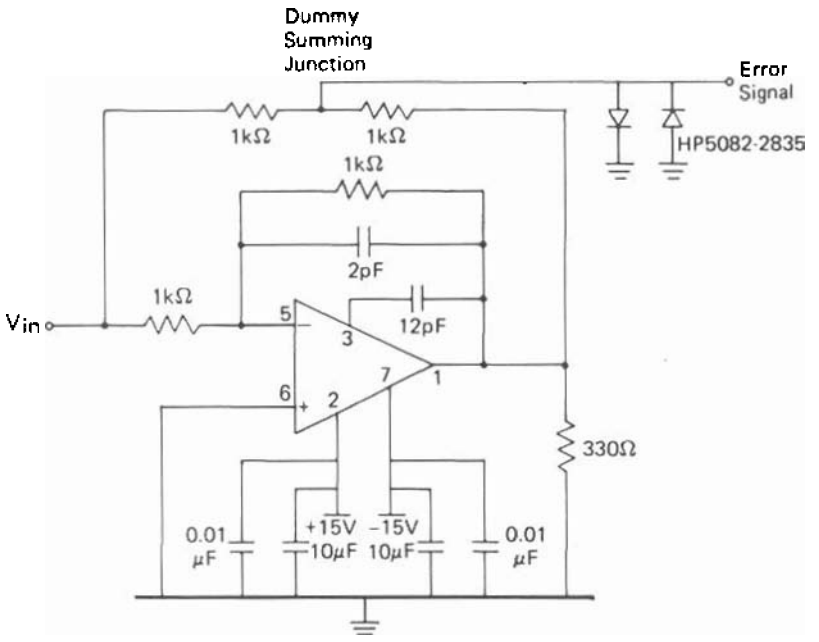
Inverting Gain of 10 Amplifier



Inverting Gain of 100 Amplifier



Settling Time Test Circuit



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