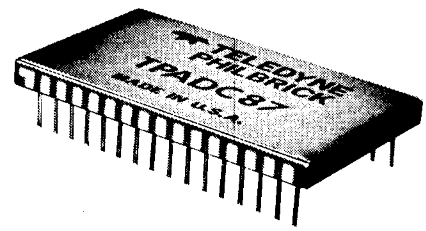
Industry Standard Industrial/Military 12 Bit A/D Converters

TPADC85 TPADC87

Versatility is the reason the ADC85 has evolved as the standard 12 bit A/D for fast commercial/industrial data acquisition applications. The device has 5 input ranges, optional input buffer, internal clock and reference, parallel and serial outputs, short cycle and clock adjust pins, and optional external accuracy adjustments. With integral linearity error guaranteed less than ± ½LSB and no missing codes guaranteed over temperature, the ADC85 is a true 12 bit performer. Its design approach and high power consumption, however, have restricted its operation to − 25°C to + 85°C. Recent advances in monolithic DAC technology have enabled ADC85 manufacturers to produce more reliable, wider temperature, lower cost devices. In Teledyne Philbrick's case, the use of a monolithic DAC not only enabled us to produce a lower power, full − 55°C to + 125°C device (TPADC87), it eliminated a number of chips in the traditional design giving us room to incorporate a unique clock circuit and a discrete comparator preamplifier. The clock circuit increases its frequency after sensing that bit 4 has been determined. This "progressive approximation" conversion technique enables the TPADC85 and TPADC87 to guarantee a maximum conversion time of 7μsec—faster than any other ADC85. The clock circuit also makes the TPADC85/87 the only ADC85's that can continuously convert 12 bits by tying the status output back to the start input.

Our own prorietary comparator preamplifier results in a comparator circuit much less prone to oscillation than available monolithics, and it gives the TPADC85/87 much cleaner digital output transitions and hence, superior repeatability. It enables us to be the only ADC85 manufacturer to guarantee differential linearity (± ½LSB max) and the only one to even specify transition noise (± 1/8LSB typical). The preamp is designed so the monolithic DAC settles into a virtual ground point. This allows the DAC to settle faster which is another reason for both our higher conversion speed and our cleaner transfer function.

The TPADC85/87 are hermetically sealed in standard 32 pin dual-in-line packages. Power consumption is typically 1200mW. For military/aerospace applications, the TPADC85/87 are available screened to MIL-STD-883, Method 5008 (add -83 to part number).



FEATURES

- 7μsec Max Conversion Time Progressive Approximation
- ± 1/2LSB Max Integral and Differential Nonlinearities
- No Missing Codes
  TPADC85 − 25°C to + 85°C
  TPADC87 − 55°C to + 125°C
- ± 1/8LSB Transition Uncertainty
- Serial and Parallel Outputs
- Optional MIL-STD-883 Screening

APPLICATIONS

- High Accuracy, High Speed Data Acquisition
- Waveform Analysis
- Medical and Military Instrumentation

TELEDYNE PHILBRICK Allied Drive @ Rte. 128, Dedham, Massachusetts 02026
Tel: (617) 329-1600, TWX: (710) 348-6726, Tlx: 92-4439

ABSOLUTE MAXIMUM RATINGS

+ 15V Supply (+ V_{CC}, Pin 28)	– 0.5 to + 18 Volts
– 15V Supply (– V_{CC}, Pin 31)	+ 0.5 to – 18 Volts
+ 5V Supply (+ V_{dd}, Pin 16)	– 0.5 to + 7 Volts
Digital Inputs (Pins 14, 21)	– 0.5 to + 5.5 Volts
Direct Analog Input (Pins 24, 25)	± 15 Volts
Buffer Input (Pin 30)	± 15 Volts
Operating Temperature Range	– 55°C to + 125°C
Specified Temperature Range	
TPADC85, TPADC85-83 (Note 1)	– 25°C to + 85°C
TPADC87, TPADC87-83 (Note 1)	– 55°C to + 125°C
Storage Temperature Range	– 65°C to + 150°C

SPECIFICATIONS (T_A = + 25°C, ± 15V and + 5V supplies unless otherwise indicated).

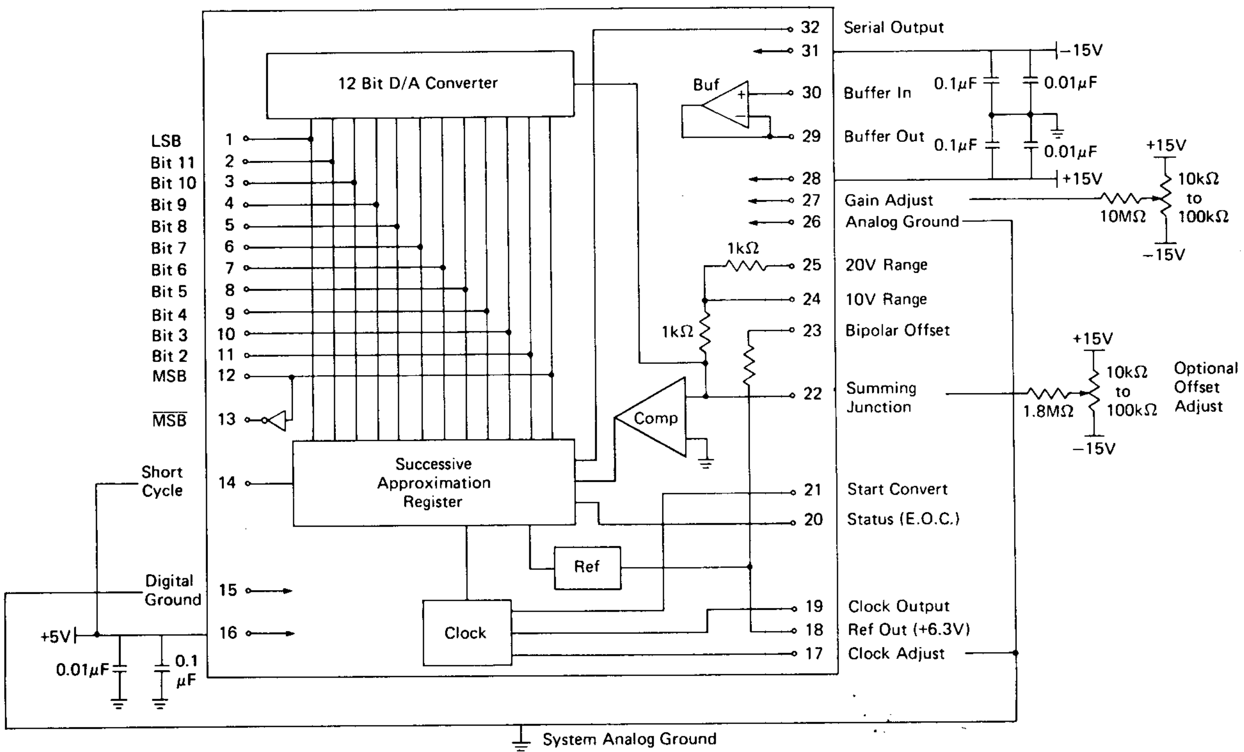
PARAMETER	MIN.	TYP.	MAX.	UNITS
ANALOG INPUTS				
Input Voltage Ranges: Unipolar		0 to + 5, 0 to + 10		Volts
Bipolar		± 2.5, ± 5, ± 10		Volts
Direct Input Impedance (Note 2): 0 to + 5V, ± 2.5V		1		kΩ
0 to + 10V, ± 5V		2		kΩ
± 10V		4		kΩ
Buffer Amplifier: Gain Accuracy		± 0.01		%
Input Impedance	10^{10}	10^{12}		Ω
Input Bias Current		± 2	± 7	nA
Offset Voltage		± 2.5	± 8	mV
Settling Time (20V Step to ± 0.01%FSR)		2		μsec
DIGITAL INPUTS				
Start Convert: Logic Levels: Logic "1"	+ 2.0		+ 5.5	Volts
Logic "0"	0		0.8	Volts
Loading (Note 3)		1		LP TTL Load
Pulse Width (Note 4)	100			nsec
DIGITAL OUTPUTS				
Output Coding (Note 5): Unipolar Ranges		CSB		
Bipolar Ranges		COB, CTC		
Logic Levels: Logic "1"	2.4	3.6		Volts
Logic "0"		0.2	0.4	Volts
Output Drive Capability (Note 6)	5			TTL Loads
TRANSFER CHARACTERISTICS (Note 7)				
Integral Linearity Error		± ¼	± ½	LSB
Differential Linearity Error		± ¼	± ½	LSB
Guaranteed No Missing Codes: TPADC85	– 25		+ 85	°C
TPADC87	– 55		+ 125	°C
Offset Error (Notes 8, 9): Unipolar		± 0.025		%FSR
Bipolar		± 0.05		%FSR
Gain Error (Notes 8, 10)		± 0.05		%
STABILITY				
Integral Linearity Drift		± 1	± 2	ppm of FSR/°C
Differential Linearity Drift		± 1		ppm of FSR/°C
Offset Drift: Unipolar		± 2	± 3	ppm of FSR/°C
Bipolar		± 4	± 7	ppm of FSR/°C
Gain Drift		± 7	± 15	ppm/°C
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 11)		6.8	7	μsec
Internal Clock Frequency (Note 12): Phase 1		1.4		MHz
Phase 2		2		MHz
Transition Uncertainty (Note 13)		± ⅛		LSB
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status)		26	40	nsec
Delay LSB Valid to Falling Edge of Status		20		nsec
REFERENCE OUTPUT				
Internal Reference: Voltage		+ 6.3		Volts
Accuracy		± 5		%
Drift		± 5		ppm/°C
External Current			200	μA

PARAMETER	MIN.	TYP.	MAX.	UNITS
POWER SUPPLIES				
Power Supply Range: ± 15V Supplies	± 14.5	± 15	± 15.5	Volts
+ 5V Supply	+ 4.75	+ 5	+ 5.25	Volts
Power Supply Rejection: + 15V Supply		± 0.3		LSB/Volt
− 15V Supply		± 0.05		LSB/Volt
+ 5V Supply		± 0.01		LSB/Volt
Current Drain: + 15V Supply		+ 20		mA
− 15V Supply		− 33		mA
+ 5V Supply		+ 81		mA
Power Consumption		1200		mW

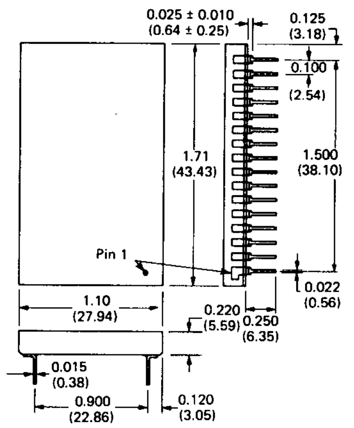
SPECIFICATION NOTES

1. The TPADC85-83 and TPADC87-83 are screened to the high reliability requirements of MIL-STD-883, Method 5008.
2. See page 8 for tips on choosing signal sources for driving fast successive approximation type A/D converters.
3. An LP TTL load is defined as sinking 20μA with a logic "1" applied and sourcing 0.36mA with a logic "0" applied.
4. Conversion is initiated on falling edge of start convert command. See Timing Diagram.
5. CSB = Complementary Straight Binary. COB = Complementary Offset Binary. CTC = Complementary Two's Complement. Serial and parallel output data have the same coding. Serial data is in Non-Return to Zero (NRZ) format. See Output Coding and Timing Diagram.
6. Specification applies for all digital outputs: parallel data outputs, serial data output, clock output, and status.
7. FSR stands for Full Scale Range and is equivalent to the nominal peak-to-peak voltage of the selected input range, i.e., FSR = 5 volts for 0 to + 5V and ± 2.5V ranges. FSR = 10 volts for 0 to + 10V and ± 5V ranges. FSR = 20 volts for the ± 10V range. For a 12 bit converter, 1 LSB = 0.024%FSR.
8. Adjustable to zero with optional external trim.
9. Offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1111 to 1111 1111 1110.
10. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000.
11. Conversion time is defined from the falling edge of the start pulse to the falling edge of the status pulse and is specified using the internal clock. See Timing Diagram. Conversion time may be shortened, with lower resolution, by short cycling and clock adjusting.
12. See Timing Diagram for explanation of progressive approximation A/D conversion technique.
13. If one were to plot the distribution of analog input voltages at which a particular output transition took place, the typical width of the distribution will be ¼LSB (± ⅛LSB).

Functional Block Diagram



Package Dimensions 32 Pin DIP



Dimensions are in inches (millimeters)

Pin Designations

Pin 1	Bit 12 (LSB)	Pin 32	Serial Output
Pin 2	Bit 11	Pin 31	−15V Supply
Pin 3	Bit 10	Pin 30	Buffer Amp Input
Pin 4	Bit 9	Pin 29	Buffer Amp Output
Pin 5	Bit 8	Pin 28	+15V Supply
Pin 6	Bit 7	Pin 27	Gain Adjust
Pin 7	Bit 6	Pin 26	Ground
Pin 8	Bit 5	Pin 25	20V Range
Pin 9	Bit 4	Pin 24	10V Range
Pin 10	Bit 3	Pin 23	Bipolar Offset
Pin 11	Bit 2	Pin 22	Summing Junction
Pin 12	Bit 1 (MSB)	Pin 21	Start Convert
Pin 13	$\overline{\text{MSB}}$	Pin 20	Status (E.O.C.)
Pin 14	Short Cycle	Pin 19	Clock Output
Pin 15	Ground	Pin 18	Ref Out (+6.3V)
Pin 16	+5V Supply	Pin 17	Clock Adjust

Applications Information

Layout Considerations

With proper grounding and bypassing, the TPADC85/87 will meet all their published performance specifications without the need for additional external components. The units' two ground pins (pins 15 and 26) are not connected to each other internally. They should be tied together as close to the package as possible and both connected to system analog ground. It is preferable to have a large analog ground plane beneath the TPADC85/87 and have pins 15 and 26 soldered directly to it. Potential differences between pins 15 and 26 and the ground of the analog signal source will result in TPADC85/87 accuracy and linearity errors. If runs to pins 15 and 26 have to be made separately, an 0.01μF ceramic capacitor should be connected between pins 15 and 26 as close to the unit as possible, and conductor runs should be as wide as possible.

Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Pin 22, the high impedance input to the internal comparator, is particularly noise susceptible. Care should be taken to avoid long runs, or runs close to digital lines when utilizing the comparator input. In bipolar operation, where pin 23 is connected to pin 22, a short jumper should be used. If optional external offset and gain adjustments are used, series resistors and adjusting potentiometers should be located as close to the device as possible.

Power supply connections should be short and direct, and all supplies should be bypassed to the same ground the converter is tied to. Bypass capacitors should be located as close to the converter as possible and should consist of one large value capacitor (1μF tantalum or larger) in parallel with an 0.01μF ceramic capacitor.

If short cycling is not used, the short cycle pin (pin 14) must be tied to +5V (pin 16) for normal 12 bit operation. For specified 7μsec conversion time, the clock adjust pin (pin 17) must be grounded.

Status Output

The status or end of conversion (E.O.C.) output will be set to a logic "1" by the rising edge of the start convert command. It will remain high during conversion, and it will drop to a logic "0" when conversion is complete. Because status rises on the leading edge of the start pulse and a conversion does not actually commence until the falling edge, conversion time must be defined as the interval between the falling edge of the start pulse and the falling edge of the status pulse. Unlike other ADC85's, the TPADC85/87 has an internal time delay (20nsec) to ensure that both serial and parallel data are valid by the time the status output drops to a logic "0". This permits parallel data transfer to be initiated by the trailing edge of the status pulse.

Start Convert Signal and Internal Clock

The start convert signal must be a positive pulse with a minimum pulse width of 100nsec. Unlike other ADC85's, the TPADC85/87 resets (MSB output goes to "0"; other bits go to "1"; status output goes to "1") on the rising edge of the start pulse. The falling edge gates on the internal clock and begins the conversion cycle. Other ADC85's perform both reset and clock enable functions on the falling edge of their start pulses. The

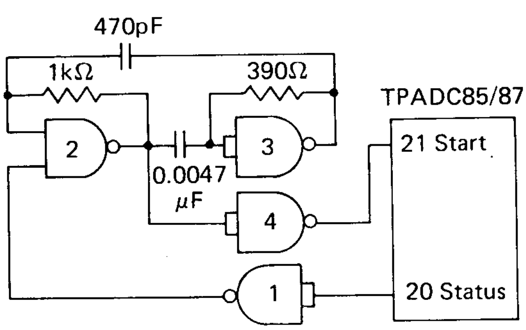
TPADC85/87 is still completely compatible with existing ADC85 sockets. For new designs however, the TPADC85/87's reset scheme allows it to continuously convert by inverting the status output and tying it back to the start convert input (see below). Other ADC85's can not do this.

The internal clock that was gated on by the falling edge of the start pulse is gated off by the status output going low at the end of a conversion. If the start convert input is brought high after a conversion has been initiated, the internal clock will be disabled halting the conversion. If the start convert input is then brought low, the original conversion will continue with a possible error in the output bit that was about to be set when the internal clock was stopped.

Continuous Converting

Unlike other ADC85's, the TPADC85/87 can be made to continuously convert by inverting and tying its status output (pin 20) back to its start convert (pin 21) input. In this configuration, status going low at the end of a conversion becomes the rising edge of the start pulse that resets the converter. When the status goes high as part of the reset action, the start pulse drops allowing the conversion to commence. The end result is that the TPADC85/87 will continuously convert and the status output will go low for approximately 60nsec following each conversion. In the figure below, the oscillator formed by gates 2 and 3 insures that the conversion process will start when the system is initially powered up.

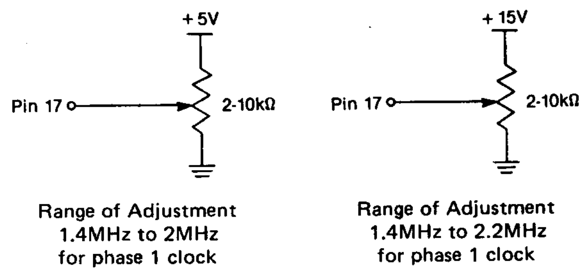
Continuous Converting for 12 Bits



Clock Rate Adjustment

See timing diagram for a description of progressive approximation type A/D conversion. The TPADC85/87's phase 2 clock frequency is approximately 1.4 times its phase 1 frequency. With the clock adjust pin (pin 17) grounded, these frequencies are preset at the factory to approximately 2 and 1.4MHz respectively. To adjust the internal clock frequencies, a ± 100ppm/°C TCR multiturn potentiometer can be connected to pin 17 as shown below. See the graph below for typical integral linearity error vs. conversion time. See short cycling for additional clock adjusting information.

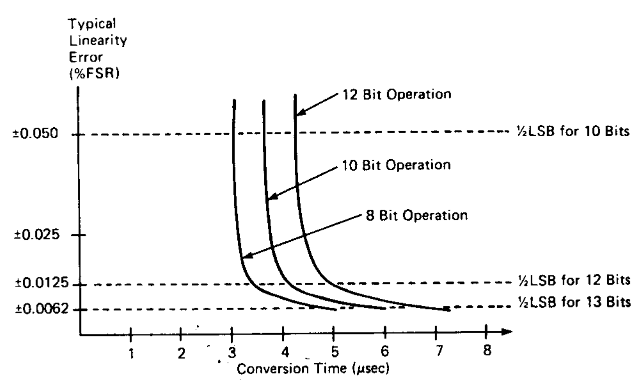
Clock Adjust Circuits



Short Cycling

For applications requiring less than 12 bits resolution, the TPADC85/87 can be truncated or short cycled at the desired number of bits with a proportionate decrease in conversion time. To truncate at n bits, simply connect the n + 1 bit output to the short cycle pin (pin 14). For example, to truncate at 10 bits, connect pin 2 (bit 11) to pin 14; converting will stop, and the status output will go low after bit 10 has been set. When short cycling, conversion times can be further reduced by increasing the internal clock frequency. The connections shown below both increase the clock rate and truncate the converter to provide the minimum conversion time for a given resolution.

Resolution Bits	12	12	10	8
Connect Pin 17 to Pin	15	16	28	28
Connect Pin 14 to Pin	16	16	2	4
Conversion Time (μsec)	6.8	4.8	3.7	3.1
Clock Freq. (MHz) Phase 1 Phase 2	 1.4 2	 2 2.9	 2.2 3.2	 2.2 3.2
Nonlinearity (typ., %FSR)	± 0.006	± 0.012	± 0.05	± 0.05



Timing Diagram

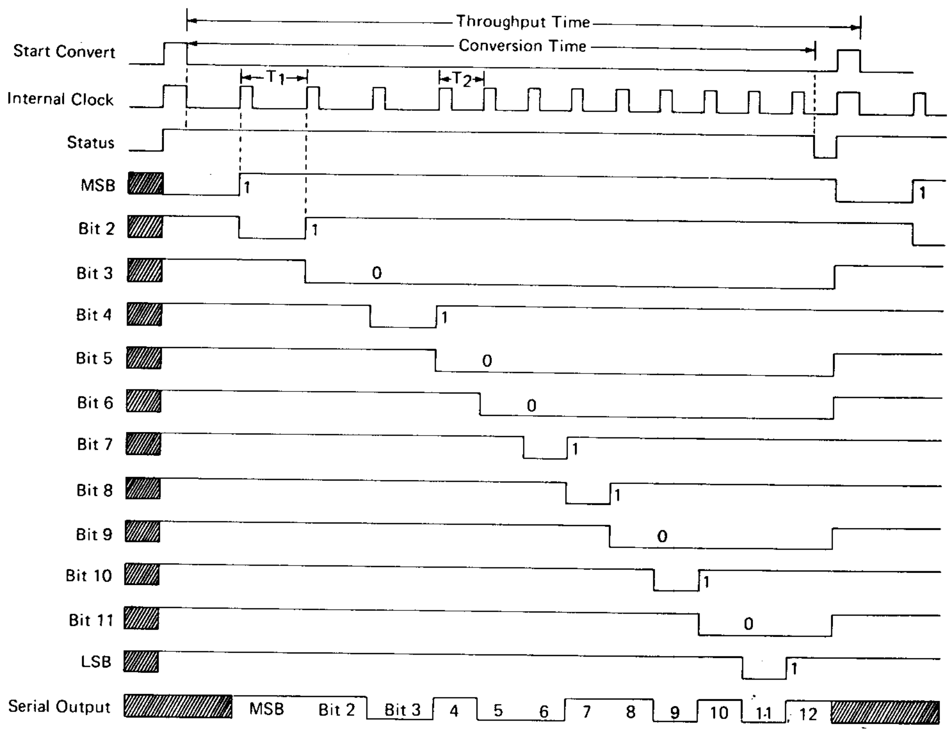
The TPADC85/87 employ the progressive approximation technique of A/D conversion. The technique is very similar to successive approximation A/D conversion except the TPADC85/87's clock begins to run faster after bit 4 has been determined. This technique results in approximately 20% faster conversion times, and it is based on the fact that an A/D's internal D/A converter takes longer to settle on more significant bit decisions than it does on less significant bit decisions. Clock acceleration after bit 4 has been set is accomplished in the following manner. The TPADC85/87's internal clock is a retriggerable monostable multivibrator. The resistor in the clock's RC timing circuit is paralleled by a second resistor that is switched in after bit 4 has been set. This results in a lower time constant and a smaller clock pulse width (higher frequency) for the remaining 8 bits.

The TPADC85/87's start pulse must be a minimum 100nsec wide, and it must remain low during conversion. The rising edge of the start pulse resets the converter (clock = "1" after 25nsec delay, status = "1" after 50nsec delay, MSB = "0", other bits = "1") and the falling edge gates on the internal clock and begins the conversion. Final bit decisions are made on subsequent rising clock edges. Parallel and serial output bits become valid on the same rising clock edges. Both become valid no longer than 40nsec after the edge. If an external clock is used, output data becomes valid no longer than 90nsec after each falling clock edge. The status output goes low gating off the internal clock approximately 20nsec after the LSB has been determined. Once a conversion has begun, a second start pulse will not reset the converter. When the TPADC85/87 is initially "powered up", it may come on at any point in the conversion cycle.

External Clock

An external clock may be connected to the start convert input. This external clock must consist of negative pulses 100 to 200nsec wide and must be at a lower frequency than the internal clock. The result is that each falling edge of the external clock turns on the internal clock for a single cycle, completing a conversion in 13 clock cycles (the internal clock is disabled whenever the start convert input is held high). When using an external clock, a start convert command is unnecessary. The converter will begin to convert when the external clock is started and will provide a continuous string of conversions with each conversion starting on the first falling edge of the external clock after the status output has gone low signaling the end of the previous conversion. When continuously converting in this manner, the status output will go low for approximately one external clock period following the completion of each conversion.

Timing Diagram

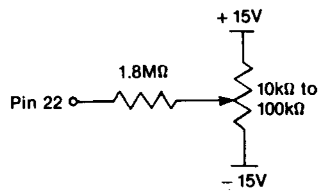


Optional Zero and Gain Adjustments

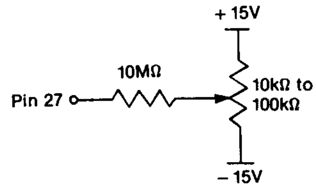
Initial zero and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warm-up, and to avoid interaction, zero should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. If these adjustments are not used, pin 22 should be connected as described in the range selection section, and pin 27 should be left open.

Zero Adjustment—Connect the zero potentiometer as shown. For unipolar ranges, apply the input voltage at which the 1111 1111 1111 to 1111 1111 1110 transition is ideally supposed to occur (+½LSB). While continuously converting, adjust the zero potentiometer until all the output bits are "1" and the LSB "flickers" on and off. For bipolar ranges apply the input voltage at which the 1000 0000 0000 to 0111 1111 1111 transition is ideally supposed to occur (−½LSB). While continuously converting, adjust the zero potentiometer until all the output bits "flicker" on and off.

Zero Adjust Circuit



Gain Adjust Circuit

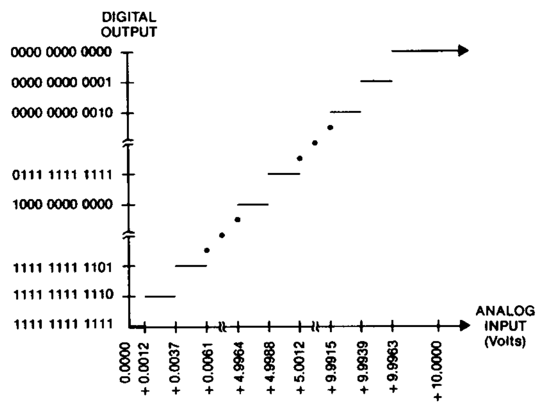


Gain Adjustment—Connect the gain potentiometer as shown, and apply the input voltage at which the 0000 0000 0000 to 0000 0000 0001 transition is ideally supposed to occur (FS-3/2LSB). While continuously converting, adjust the gain potentiometer until all the output bits are "0" and the LSB "flickers" on and off.

Digital Output Coding

Because of the inherent uncertainty associated with quantizing an analog signal, the only points along an ADC's input/output transfer function that accurately describe the function are the transition voltages—the analog input voltages at which the digital output changes from one code to the next. The sketch to the right shows the ideal input/output transfer function for the TPADC85/87's 0 to +10V input range. The table below lists five of the most important transition voltages for each of the TPADC85/87's five input ranges. 1111 1111 111* indicates the TPADC85/87's digital output ideally changes from 1111 1111 1111 to 1111 1111 1110 (or vice versa) at the input voltage listed for the input range selected. **** **** **** signifies the center of an input/output range where the digital output changes from 1000 0000 0000 to 0111 1111 1111. CSB = Complementary Straight Binary. COB = Complementary Offset Binary. CTC = Complementary Two's Complement—this coding is achieved using the $\overline{MSB}$ output on bipolar input ranges.

Ideal Transfer Function 0 to +10V Range



Analog Input (DC Volts)						Digital Output Transition		
Input Range	0 to +5V	0 to +10V	±2.5V	±5V	±10V			
Logic Coding	CSB	CSB	COB, CTC	COB, CTC	COB, CTC			
LSB Size (12 bits)	1.22mV	2.44mV	1.22mV	2.44mV	4.88mV	MSB		LSB
Transition Voltage	+4.9982	+9.9963	+2.4982	+4.9963	+9.9927	0000	0000	000*
	+4.9969	+9.9939	+2.4969	+4.9939	+9.9878	0000	0000	00*0
	+2.5006	+5.0012	+0.0006	+0.0012	+0.0024	0111	1111	111*
	+2.4994	+4.9988	−0.0006	−0.0012	−0.0024	****	****	****
	+2.4982	+4.9963	−0.0018	−0.0037	−0.0073	1000	0000	000*
	+0.0018	+0.0037	−2.4982	−4.9963	−9.9927	1111	1111	11*1
	+0.0006	+0.0012	−2.4994	−4.9988	−9.9976	1111	1111	111*

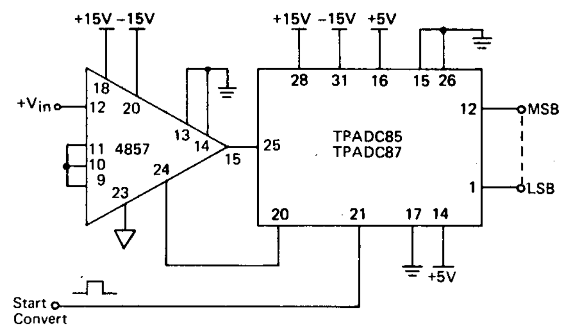
Input Range Selection

Pin Connections		Input Voltage Range				
		0 to +5V	0 to +10V	±2.5V	±5V	±10V
Normal Input	Input Impedance (kΩ)	1	2	1	2	4
	Connect Pin 23 to Pin	26	26	22	22	22
	Connect Pin 25 to Pin	22	Open	22	Open	Input
	Connect Pin 30 to Pin	26	26	26	26	26
	Connect Input to Pin	24	24	24	24	25
Buffered Input	Input Impedance (MΩ)	10^4	10^4	10^4	10^4	10^4
	Connect Pin 23 to Pin	26	26	22	22	22
	Connect Pin 25 to Pin	22	Open	22	Open	29
	Connect Pin 29 to Pin	24	24	24	24	25
	Connect Input to Pin	30	30	30	30	30

Using a Sample-Hold Amplifier with the TPADC85/87

Sample-hold (S/H) and track-hold (T/H) amplifiers can be used with the TPADC85/87 in a number of different configurations. There are three major considerations when using S/H's with SA type A/D converters. First, the S/H's output impedance should be very low compared to the A/D's input impedance (normally 1 to 10kΩ) at frequencies up to 5 times the A/D's clock frequency. Second, the S/H output should be able to fully recover from current transients in less than 1 A/D clock period. These requirements are due to the fact that as the A/D's internal DAC settles just prior to each output bit being determined, the S/H output may be required to sink and source high frequency current components, and changes in its output voltage will cause system accuracy errors. The third consideration is the S/H spec called sample-to-hold settling time (transient settling time). As you switch a S/H from the sample to the hold mode, an output transient usually occurs, and one must be sure this transient has settled before the A/D makes its final decision on the MSB.

If the TPADC85/87 is being used in a single conversion mode with an external start pulse, the S/H can be driven directly (or inverted) from the A/D's status output. The status output changes state when the converter receives a convert command, and this change can drive the S/H from the track to the hold mode. The change in state of the A/D's status output at the end of the conversion can put the S/H back into the track mode. The diagram above illustrates a TPADC85/87 mated with a Teledyne Philbrick 4857 (1μsec max acquisition time, 500nsec max sample-to-hold settling time) in this manner. Since the TPADC85's MSB output is not set to its final value until one clock period (approximately 700nsec) after a conversion begins, the 4857's sample-to-hold transient will be completely settled, and no extra precautions are necessary.



If the TPADC85/87 is used in a continuous convert mode, its status output goes low for approximately 60nsec following each conversion. This is not enough time for any S/H to acquire a new signal to ±0.01%, and it becomes necessary to use a one-shot to generate the S/H acquisition command and the next start convert signal. The diagram below shows such a scheme using a Teledyne Philbrick 4860 (200nsec max acquisition time, 100nsec max sample-to-hold settling time). See the 4857, 4860, 4189, and TP5210 data sheets for additional tips on mating S/H's and A/D's.