THE LIGHTNING EMPIRICIST

Advocating electronic models, at least until livelier instrumentalities emerge

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FOREWORD

In this second issue of the recently resuscitated LIGHTNING EMPIRICIST, we offer several discussions of procedures in which operational amplifiers are included in circuits which perform in a discontinuous fashion: which are subject to abrupt changes in character. We hope these treatments are useful. At the same time we hope not to give the impression that all analog operations are discontinuous, however necessary and valuable these may be in some cases.

The fact is that, in a large and familiar class of analog instruments, operational amplifiers are applied in a completely continuous fashion, with no "switching" operations at all – whether originated from without or from within. Consider, as a single-amplifier example, a time-wise differentiator. Acting continuously in an on-line data processing role, such a machine may perpetually provide the derivative of a variable with respect to time. It will ordinarily require no logical alterations of structure to perform successfully. Similarly, this is the case for higher derivatives, if you believe in them, and for a great many more sophisticated filtering functionals.

Traditionally an operational integrator must be "set" and/or "held" by means of discontinuous actions. As usual, however, tradition is poorly informed. In a host of integrator applications, ancient and modern, no discontinuous alterations in circuitry need be involved once the power has been turned on. Granted that a lone integrator is an unstable device, presuming in particular that it is subjected to a prescribed input function. An open-ended chain of unmanipulated integrators is obviously even less stable. But observe, for instance, the operational circuit which provides the integrative term in an automatic regulator. This can run unattended in perpetuity (although of course switching faculties may make it more adept). The reason is that then the input is dynamically related to the output in a special manner, i.e., a servo loop.

Again, if integrators are applied in building a model of a dynamic system, no discrete preparatory actions are really required in the operational circuitry as long as the system being modelled is stable. Since the condition of stability is generally the one being sought, the absence of switching facility is manifestly a mild limitation. Initial conditions need not even be imposed in the traditional way, since either transient or spectral perturbations may be supplied from outside the model, the latter being otherwise free and self-determining. These then are a few "alogical," ungated, continuously-acting operational amplifier usages to break the spell.

In the analog instrument of the Pease article, presented on another page of this journal, wherein one operational amplifier serves for a compounded crossing detector and monostable multivibrator, discontinuous behavior is rife and requisite. We only comment that it is not a primary purpose, in promulgating this artifice, to reduce our sales of amplifiers but rather to extend their usefulness to new areas by demonstrating their unexpected versatility.

Since some Hybrid Operational Amplifiers are presented herein, in which integrated circuitry may be combined with "discrete" circuit elements, we might include a few cautionary remarks on terminology. The term *Hybrid* here refers narrowly to this combination. It should not be confused with the frequently-used alternative meaning, within the same general area of technology, whereby a hybrid computational structure comprises a combination of analogical plus digital subsystems, variously permuted.

As to *Discrete* one must not confound this usage (which means that each circuit element is designed and assembled as an individual component – or chip) with that in which the same term refers to discontinuous and separated functions of time, as in logical or numerical operations as opposed to continuous ones. Thus we observe that it is appropriately discreet (*sic*) to regard such terms carefully within their contexts.

Your comments on the March, 1969, issue of the *LIGHTNING EMPIRICIST* have been most helpful. Please continue sending your suggestions, contributions and corrections, as well as address changes and requests for extra copies to

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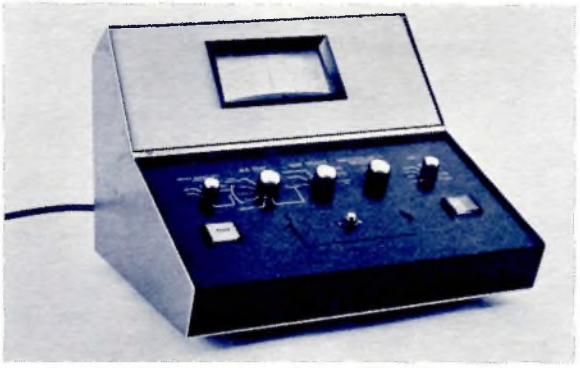
SYNCHRONOUS DEMODULATION METHOD FOR DYNAMIC TESTING OF OPERATIONAL AMPLIFIERS

R.A. Calkins & E.L. Maddox



Model 5102 Operational Amplifier Tester

INCORPORATING SYNCHRONOUS DEMODULATION

Static tests for operational amplifiers can be readily performed with the aid of low cost testers, but similar examination for dynamic characteristics presents a considerably harder problem. The test instrument is required to present accurate results for "open-loop gain," common-mode range and rejection, output swing, and power supply rejection. The user demands a unit that is easy to operate and possesses direct readout capability. To satisfy these standards with a low-cost instrument, a new synchronous demodulation method of dynamic test measurement was developed and incorporated into Model 5102 Philbrick/Nexus Operational Amplifier Tester.

In the new synchronous detection method, square wave signals are applied to the amplifier connected in a stable closed-loop mode and thus assured of operation in its linear region. In most other test methods, the output depends on the gain of the Amplifier Under Test (AUT) and when large signals are applied, there is a chance that the device will be operating out of its linear region.

Earlier Test Methods

The advantages of the synchronous detection method are best demonstrated by first considering the drawbacks of three earlier test schemes.

In the first method, an auxiliary amplifier is used to keep the amplifier under test zeroed for offset. To accomplish the zeroing, the circuit of Fig. 1 has two resistors, R_f and R_S. The source resistor, R_g, is made large in comparison with R_S to assure that only a small signal is applied to the circuit under test. Feedback capacitor, C_1 around the auxiliary amplifier, essentially opens the loop at the input signal frequency, which is typically in the range of 10 to 30 hertz. The output voltage and gain of the amplifier under test for this circuit are:

$$e_o = e_{in} \frac{R_s}{R_g + R_s} \cdot \frac{R_2}{R_1 + R_2} \cdot A_o \quad \text{where:}$$

$$A_o = \frac{e_o}{e_{in}} \cdot \frac{1}{S} \quad \text{and} \quad S = \frac{R_s}{R_s + R_g} \cdot \frac{R_2}{R_1 + R_2}$$

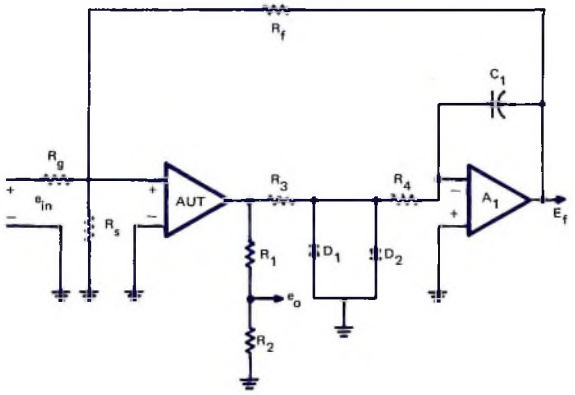


Fig. 1. Gain Measurement

To determine the open-loop voltage gain for an integrated circuit operational amplifier, A_1 must keep the amplifier under test (AUT) zeroed for offset via resistors R_f and R_S. However, because C_1's value must be extremely large, the circuit is impractical.

If the input and output voltages of the amplifier under test are displayed as a Lissajous pattern the slope of the line, when properly scaled, represents the open-loop gain.

The two diodes clip the output of the amplifier so that no input offset voltage is induced by an unsymmetrical output swing if the amplifier is overdriven. Such a condition can be observed on the oscilloscope and the linearity of the amplifier under test can be evaluated.

This method thus has the advantage of displaying gain, output swing and linearity simultaneously, with the additional benefit that all signals are high level, which eliminates any noise problems. However, it has some serious disadvantages.

First, the output level is directly dependent on the open-loop gain, which makes programming of output test conditions extremely difficult.

With the high gain, internally damped IC amplifiers now available, capacitor C_1 must have an extremely large value to open the loop adequately at the signal frequency.

The R_g–R_S attenuator must be very accurate and variable if amplifiers with wide variations in parameters are to be tested. Hand programming is mandatory. Finally, the readout device–the oscilloscope–is not easily adaptable to a direct-reading meter (nor is it easily calibrated or interpreted).

The second method, Fig. 2, is far simpler than the first but has all its drawbacks. It consists of a simple feedback circuit with an attenuated input applied to the amplifier under test. For an ac signal, the gain will be

$$A_o = \frac{R_g + R_s}{R_s} \cdot \frac{e_o}{e_{in}}$$

This circuit does not allow the amplifier under test to be overdriven in a predictable way as the square wave output tends to rebias the IC, changing its response.

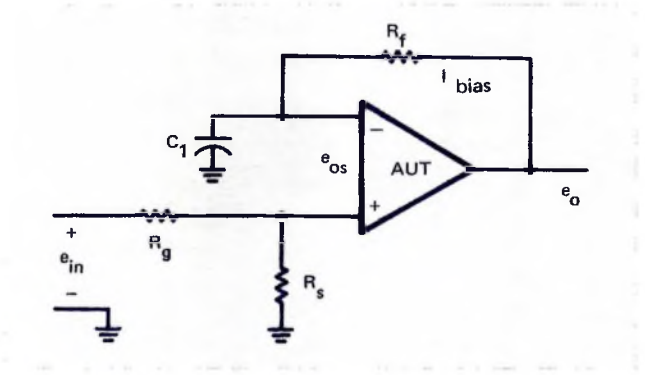


Fig. 2. Voltage Gain

Output e_o at dc is equal to the input offset voltage plus the drop across the feedback resistor, I_{bias} R_f. Circuit cannot be overdriven because the output tends to rebias the IC, thus changing its open-loop response.

The third method, given in a new military standard, is also simple; see Fig. 3. The signal is applied to the amplifier under test through a voltage divider, coupling capacitor, and feedback resistor, R_1, with a shunted resistor from one terminal of the amplifier to ground. Under the condition that

$$\frac{(A_o + 1)\ (R_3 \| R_4 - j X_{c_1})}{R_1} < 0.1,$$ the open-loop gain is

$$A_o = \frac{e_o}{e_s} \cdot \frac{R_3 + R_4}{R_4} \qquad (R_3 >> R_4)$$

The imposed condition requires that the closed-loop gain approach the open-loop gain within 90%. Thus the stabilizing effect of the feedback has been lost, making the output signal depend on the gain again.

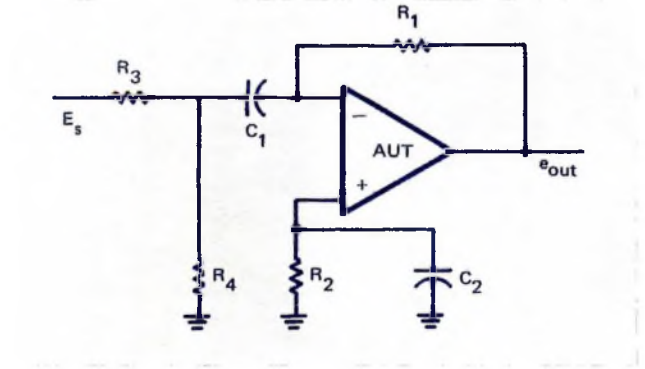


Fig. 3. MIL Std Gain Test

Closed-loop gain must approximate the open-loop gain by 90% for this test setup to be effective. The output depends on gain, and C_1 may be impossibly large.

The method is thus an impractical way of characterizing the open-loop response of an amplifier. For example, suppose that the amplifier has an open-loop gain, A_{vo} of 100,000 volts/volt, a unity gain-bandwidth product, f_t of 1 megahertz, and a feedback resistor, R_1 of 10 kilohms. For conditional equation to hold, $R_3 \| R_4 - j X_{c_1} \leq 0.01$

Suppose R_3 is much greater than R_4 so that the parallel combination is approximately equal to R_4, and that

$X_{c_1} \leq 0.1\ R_4$ then

$R_4 \leq 0.01$ ohm and $X_{c_1} \leq 0.001$ ohm

With a 6 decibels/octave roll-off, the first open-loop break occurs at a frequency of 10 hertz. Thus to get an accurate determination of the gain, the measurement must be performed at or below this frequency. At 10 hertz, the value of C_1 must be

$$C_1 = \frac{1}{2\pi \cdot 10 \cdot 0.001} = 16 \text{ farads}$$

which is hard to come by.

Synchronous Detection System

In the synchronous detection system the signal input to the test circuit is a square wave produced by switching between two stable dc references. The output signal from the test circuit is amplified with precision, and band-limited to reject dc drift, very low frequency noise (flicker), and the high frequency noise.

The amplified signal is demodulated or converted back to a dc signal with a peak-to-peak detector switching in synchronism with the input signal. Because synchronous demodulators provide good signal-to-noise ratios, low level signals on the order of microvolts can easily be detected.

The operation of a synchronous detection system in the measurement of open-loop gain is detailed in Fig. 4.

The output of the amplifier under test is

$$e_{o,\,p\text{-}p} = \frac{R_2}{R_1} \cdot 2|V_{ref}|$$

As the amplifier is running in a closed-loop mode, a gain-error signal (e_ϵ)

$$e_\epsilon = -\frac{e_o}{A_o}$$

appears between the negative input terminal and common, where A_o is the open-loop gain of the amplifier under test.

This signal e_ϵ is ac coupled, and amplified to an appropriate level before being demodulated by switching circuit S_2. Capacitor C_1 charges in a negative direction with respect to ground on one half cycle. On the next half cycle, C_2 charges in a positive direction.

After a few cycles, the dc signal across C_2 is equal to the peak-to-peak value of the gain error signal multiplied by the appropriate ac gain. The dc signal is

$V_{dc} = e_\epsilon \cdot A_1$ where A_1=gain of the ac amplifier.

Thus:

$$A_o = A_1 \cdot \frac{R_2}{R_1} \cdot \frac{2|V_{ref}|}{V_{dc}}$$

This dc signal is used to drive a logarithmic amplifier for direct readout in decibels on a panel meter.

The basic circuit requires some precautions. The switching signal must be of low enough frequency that the transient spikes on the detected signal introduce minimal error. The maximum repetition rate will be determined by the low-frequency open-loop characteristics of the amplifier under test. Some form of protection is needed for the input terminals of the amplifier under test.

The ac amplifier must be able to pass the low frequency square waves encountered and its output impedance must be relatively low to allow C_1 and C_2 to charge quickly. Finally, the dc follower must have a very high impedance input (preferably a field-effect transistor type) not to discharge C_2 on alternate half cycles.

The actual circuitry eliminates the effect of transient spikes by timing the control of S_2 such that it only closes its shunt or series path during the last half of each half cycle of the test signal. This timing prevents the transients from charging C_1 and C_2.

The synchronous switch shown as S_2 consists of two junction field-effect transistors operated in a shunt-series chopper configuration. The use of a good FET input operational amplifier for the follower allows signals ranging in level from a few millivolts to 10 volts to be demodulated accurately. The only significant error of this circuit is that produced by the follower's offset and drift. This circuit has a wide dynamic range used to advantage to drive a stable logarithmic amplifier and display.

Common-mode rejection ratio (CMRR) measurements are made dynamically with the synchronous detection system. In this test the AUT is connected in a differential amplifier circuit containing a precisely trimmed set of resistors. The square wave signal drives the common inputs while the output is detected by the synchronous detector. A known input level and known differential-mode gain permit calibration in terms of test circuit output. The common-mode rejection is

$$CMRR = \frac{e_{cm}}{\Delta E_{os}} = \frac{e_{in}}{e_{out}} \cdot A_{dm}$$

The dc output from the detector is fed to a logarithmic amplifier, producing a linear readout scaled in db.

Power supply rejection ratio (PSRR) is tested in the synchronous detection system by applying the square wave to modulate a power supply and observing the effective ΔE_{os} by measuring the output of the AUT operating in a fixed-gain circuit. As before, the synchronous detector output is converted for db readout by a logarithmic amplifier.

IC Operational Amplifier Tester Model 5102 incorporates this test method for all dynamic tests. It performs the tests mentioned along with all basic dc parameter tests. Ranges for the various measurements are suitable for IC, hybrid, and discrete operational amplifiers. The low I_{bias} levels of FET input amplifiers can be measured (to 10pA F.S.) with the use of a low-current test socket.

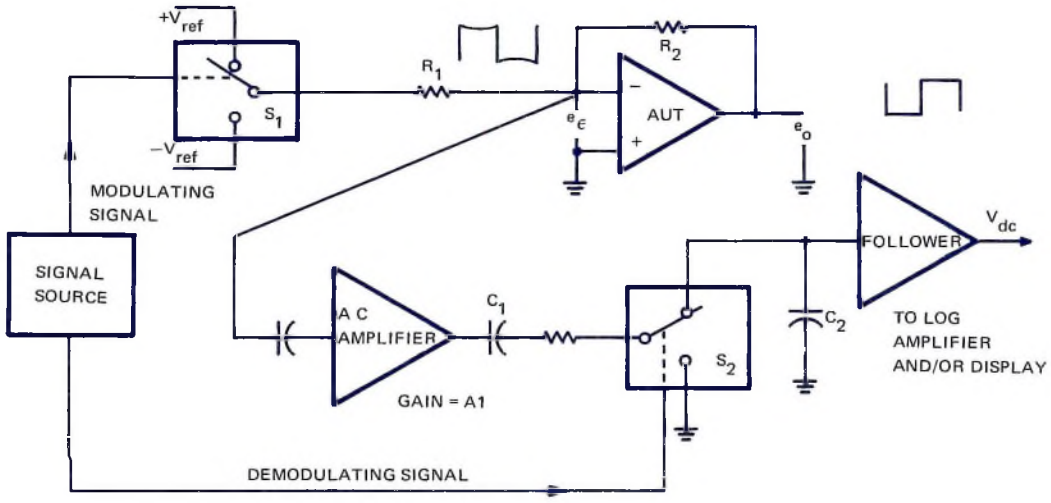


Fig. 4. Synchronous detection system

A drive signal is generated by switching circuit S_1. The error voltage, e_ϵ, developed at input of the amplifier under test is amplified then demodulated by switching circuit S_2, which operates synchronously with S_1.

THE 4850 GATED OPERATIONAL AMPLIFIER

A NEW UNIVERSAL FUNCTION MODULE

R.J. Gurski, Sc.D.

Background

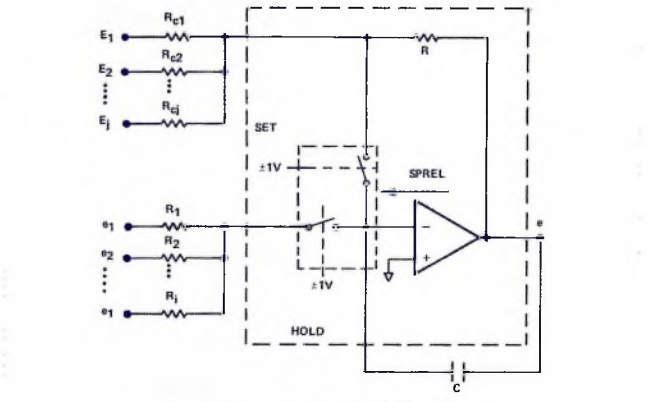
The 4850, with a few appropriate external components and logic signals, can perform the operations of integration, summation, tracking, holding, reset (to a constant or time-varying initial condition), and switching. One can see that the name given the 4850 does not really come close to describing its abilities. Other names might have been: 3-Mode Integrator, Track-and-Hold Operator, Gated Integrator, or Controlled Integrator. These names do describe some of the 4850 features but, in general, are far too restrictive. As we shall see, the most essential subsection of the 4850 is what is called a *Gated Operational Amplifier** and consequently we have elected to call this module, with all of its other features, by that name.

Evolution

A 3-mode integrator is shown in Fig. 1 using a Philbrick/Nexus Research SPREL set-hold relay pair. One notes that reset is accomplished with a speed controlled by the time constant RC; hence, R must be low for fast reset (or track), which could result in amplifier and/or source device overload. Furthermore, the HOLD switch must be open during the SET operation. Mechanical relay contact bounce, delay, and dwell time can cause erratic starting of the integration or holding operations—a particularly serious problem for the analog computationalist who may be using many such integrators, hopefully in synchronism, at high repetitive speeds. For the DTL and TTL logicians, but not the analog enthusiasts, the ± 1 volt logic requirements of the SPREL are somewhat less than desirable.

Fig. 2 is a block schematic of the 4850 with the external components necessary to emulate the functions (but not performance) of the SPREL system of Fig. 1. Three changes shown in Fig. 2 make the 4850 better than the SPREL system:

1. A unity gain (gated) amplifier, A_2, isolates the secondary initial condition and/or track summing point from the main amplifier,
2. Fast FET electronic switches replace mechanical relays, and
3. Comparators, C_H and C_S, permit differential logic, and eliminate the ± 1 volt logic drive requirement of the SPREL.



SET operation: SET closed, HOLD open

$$-e = \frac{\sum_j \frac{R}{R_{cj}} E_j}{RCP + 1}$$

RUN operation: SET open, HOLD closed

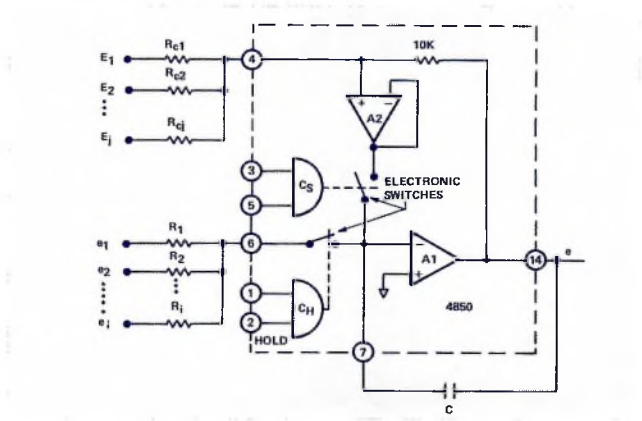
$$-e = \frac{1}{CP} \sum_i \left(\frac{e_i}{R_i}\right) + \sum_j \left(\frac{R}{R_{cj}} E_j\right)\Bigg|_{t=0}$$

HOLD operation: SET open, HOLD open

e = value of voltage on C at moment of HOLD command

$$P \equiv \frac{d}{dt}\ ; \qquad \frac{1}{P} = \int dt$$

Fig. 1. A SPREL Controlled Integrator



RESET or TRACK operation:

RESET closed, HOLD open or closed

$$-e = \sum_j \left(\frac{10K}{R_{cj}} E_j\right)$$

RUN operation: SET open, HOLD closed

$$-e = \frac{1}{CP} \sum_i \left(\frac{e_i}{R_i}\right) + \sum_j \left(\frac{10K}{R_{cj}} E_j\right)\Bigg|_{t=0}$$

HOLD operation: SET open, HOLD open

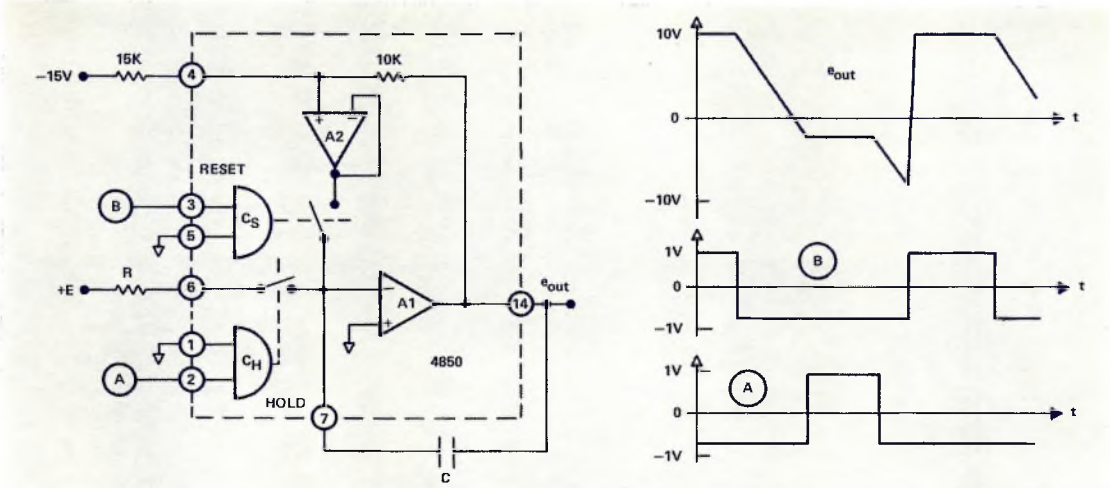
e = value of voltage on C at moment of HOLD command

$$P \equiv \frac{d}{dt}\ ; \qquad \frac{1}{P} = \int dt$$

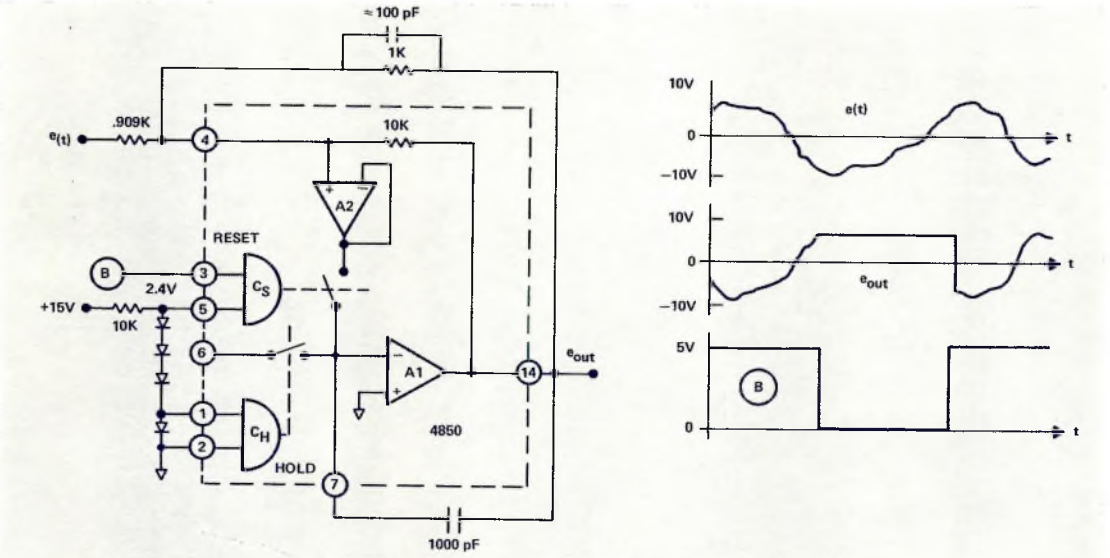
Fig. 2. A 4850 Controlled Integrator

*See Philbrick/Nexus Applications Manual, pp. 61, 62.

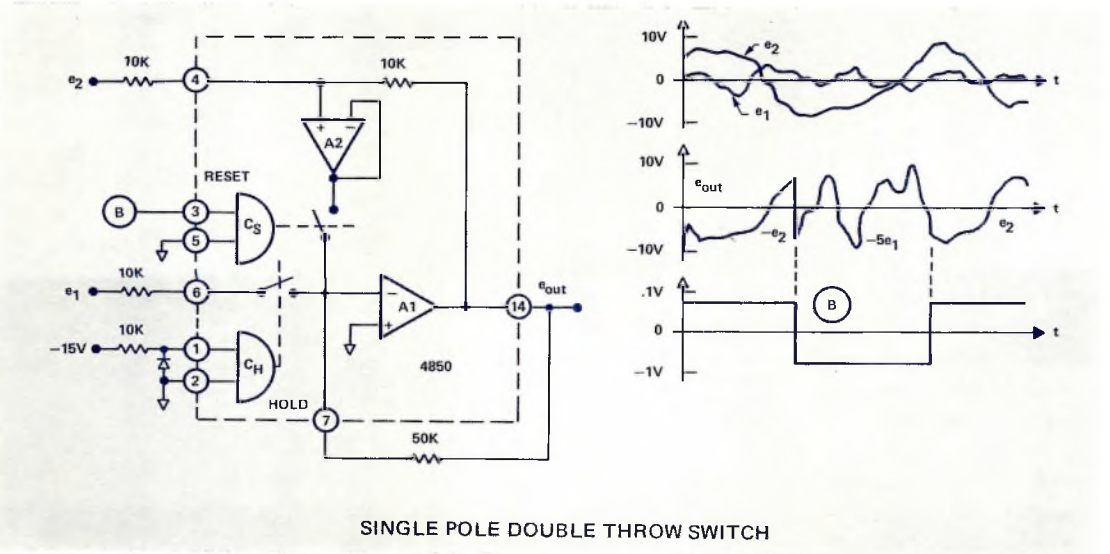
APPLICATIONS OF THE 4850



THREE-MODE INTEGRATOR



FAST TRACK-AND-HOLD



SINGLE POLE DOUBLE THROW SWITCH

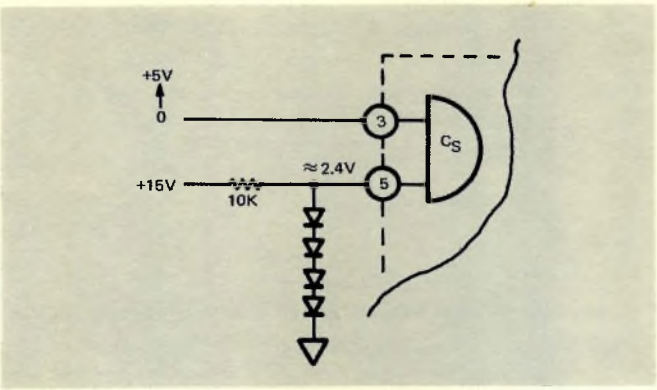
The basic function of amplifier A2, when gated on, is to isolate the initial condition summing point from the main amplifier summing point. Decoupling the 10kΩ reset feedback resistance from the main amplifier (A1) feedback capacitance in this manner makes the speed of response in reset and/or track mode independent of the RC time constant limitation of the SPREL system.

Theoretically, A2 should be designed to provide all the current necessary to slew the voltage on the capacitor at the rate-limit value of A1. This, however, would be impractical for large capacitance because of the magnitude of the currents required. Consequently, A1 has been designed to run "bang-bang" at approximately 20 milliamperes output current whenever the reset summing point error at terminal 4 exceeds a predetermined absolute value, and to run proportionally when below this value. A constant 20 milliamperes of current will cause a 1000 pF computing capacitor (the smallest recommended) to slew at 20 v/μsec, which is approximately equal to the rate limit of A1. For larger capacitances the output waveform during reset will, therefore, ramp at a rate determined by 20 milliamperes until the reset summing point error falls below the predetermined value whereupon linear operation commences and the waveform becomes exponential. This method of operation permits the fastest possible reset with a reasonably limited current supply.

With a 10kΩ reset feedback resistor and other components not shown in Fig. 2, the 4850 is guaranteed to be stable for rated load and any main amplifier feedback impedance, capacitive *or* resistive. Unfortunately, guaranteeing universal stability does degrade the reset and/or track speed implied by 20 milliamperes of current for capacitors smaller than 10,000 pF. Luckily, for the fast-trackists, there is a fix – simply shunt the 10kΩ resistor by, let us say, 1kΩ between pins 4 and 14, and appropriately modifying the R_{cj} input resistor(s). In addition to this, one must also provide in shunt with this feedback resistor, a small stabilizing capacitance. Choose a value which gives good transient response to a squarewave applied to the track input resistor.

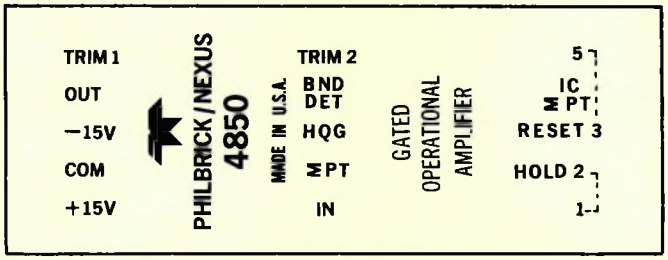
In the SPREL system, the HOLD switch must be open during the reset or track operation. Not so for the 4850! Input current being supplied to A1 by e_i is simply absorbed. Therefore, an analog computer composed of 4850's can be run in the so-called "rep-op" mode by means of the SET switch alone, with the HOLD switch being used only when HOLDing is required during an integration. In the typical Track-and-Hold operation, only the SET switch need be manipulated since all e_i are zero (no connection), and consequently integration without cause will not occur.

The switch drivers are actually comparators, of modest performance, which will accommodate most types of digital logic in addition to being able to compare two analog signals. For instance, 0 to +5 V logic can be set up as follows.



An ordinary resistor-divider network will work just as well. Complementary logic is obtained by simply reversing the connections to pins 3 and 5.

As in the past, Philbrick/Nexus Research has always endeavored to make the use of its products as self-evident as possible. Because of the comparator type logic of the 4850, and the consequent difficulty of deciding what is ON or OFF, or TRUE or FALSE, we have adopted a logic convention which we hope will allow the user to set up the circuit correctly the first time with only the unit in hand and a small amount of mental memory; and without resorting to the instruction manual. The icon the 4850 presents to the user is:



The RESET terminals are 3 and 5; and the HOLD terminals are 1 and 2. Furthermore, note that the words HOLD and RESET are adjacent to terminals 2 and 3, respectively.

On an ordered scale, a given state shall be defined as TRUE relative to all possible states below it, and FALSE relative to all possible states above it. Given a signal and a reference, the signal will be TRUE when it ranks above the reference and FALSE when below. If we rank positive voltage higher than negative voltage, then a voltage signal is TRUE whenever it is greater than the reference. For example, +2.0 volts is TRUE relative to a reference of +1.0 volts. Let us call the terminals 2 and 3, which are labeled HOLD and RESET, the input terminals, and 1 and 5 the HOLD and RESET reference terminals, respectively. Using the HOLD as an example, the rule is this: If a TRUE voltage (relative to the reference) is applied to terminal 2, (the one marked HOLD), the HOLD condition will be TRUE (i.e., enforced). If a FALSE signal is applied, the HOLD condition will be NOT TRUE (i.e., FALSE, and not enforced). The same applies to the RESET terminal. In summary, applying TRUTH to the labeled terminal will enforce the labeled condition upon the 4850.

An obvious feature is that complement logic is obtained by simply interchanging the role of the two comparator inputs. Furthermore, the reference signal need not be constant and can be used for comparing two analog signals or inhibiting digital signals.

Another feature, not shown in Fig. 2, is a low leakage feedback bound for the main amplifier, which also provides an auxiliary output signal on pin 9 whenever bounding occurs at approximately ±10.5 volts.

A SPECIAL MULTIVIBRATOR

R.A. Pease, Staff Engineer

The monostable multivibrator is a well-known circuit function for generating a timing pulse of a constant width after being triggered. The crossing detector is a circuit function for generating a step when a signal crosses a certain reference level. Often operational amplifiers are used to implement these functions, as is also discussed in the Philbrick/Nexus Applications Manual (Sections III .21 and II .41, respectively).

Recently, we had the privilege of talking with an engineer who needed to generate an accurate pulse of constant width after a zero-crossing. This can be done easily by cascading two standard circuits, but the space and cost requirements made it undesirable to specify a circuit with two operational amplifiers. However, the standard multivibrator circuit in Fig. 1 is triggered only by a sharp wavefront, such as the output of the comparator circuit of Fig. 2, and not by a dc level or crossing.

So at first we dismissed as "wishful thinking" his desire to get the job done with just one operational amplifier, and we suggested certain component values and amplifier types to do his job. But then we were challenged by the problem, and, after studying it closely, we decided that we could do it after all!

The engineer's requirement was to generate a 180 msec (±2%) pulse after the input level crossed +1.000 volt (with an accuracy of just a few millivolts), over a moderate temperature range. In the circuit of Fig. 3, a single QFT-5 will do the job. Starting at $V_{in} = 0$, the amplifier's minus input will be at 0 volts, the positive input will be at approximately –1 volt, and the output will saturate at –13 volts.

When the input signal rises to +1.000 volts (trim P1 for this set-point), the amplifier's + input voltage will cross and exceed its – input voltage, and the output will promptly switch from –13 volts to approximately +12 volts saturation. Up to this point we have had a simple crossing detector, with CR5 and CR6 inactive (open-circuit, back-biased). Now CR6 will conduct and establish CR5 as a low-impedance reference level, against which the – input voltage will be compared. (The – input voltage will ramp up toward +6 volts as C_T is charged up through R4, similar to the action in the circuit in Fig. 1).

The moderate current through CR6 is large enough to make the zener voltage of CR5 stable and independent of V_{in}, even if V_{in} should be as large as ±10 volts or 20 volts!

Thus the positive feedback through CR6 converts this circuit into a multivibrator whose action will be completely independent of the signals and components that are involved in the crossing-detector function.

After the – input voltage rises above the + input voltage, the output will switch to –13 volts again, and stay there until the circuit is triggered again. The time elapsed while the output is high will be

$$T \cong \frac{R4 \bullet C_T \bullet (V_z \text{ of CR5})}{(V_{out}, \text{Max}) - 1/2\,(V_z \text{ of CR5})}$$

or in this case,

$$180 \text{ msec} = \frac{300\text{k}\,\Omega \bullet 1\,\mu\text{f} \bullet 6\text{V}}{13\text{V} - 3\text{V}}$$

Of course, it is most economical to trim R4 so that a low-cost 20%-tolerance capacitor can be used for C_T, or a low-cost 10%- or 20%-tolerance zener diode for CR5. However, a low temperature coefficient and stable characteristics may be desirable for R4, C_T, and CR5.

Now that V_{out} has returned to its stable state, the circuit will complete its cycle and be ready again for triggering as soon as the – input voltage returns to 0 volts. The time required for that will be

$$t \cong \frac{R5 \bullet C_T \bullet (V_z \text{ of CR5})}{(V_{out}, \text{Min}) + 1/2\,(V_z \text{ of CR5})}$$

If R5 is a low value, that will be a short time, or if a long delay is desired, R5 can be a high value. But this time must be planned so that the signal will have fallen back below +1 volt dc before T + t have elapsed, or else the circuit will re-trigger falsely and, in fact, free-run. Fortunately, the engineer's requirement was easily fulfilled, as it was known that V_{in} would fall back to 0 volts very shortly after the crossing had occurred. In the case shown, $t \cong 12$ milliseconds, so that the circuit will be ready for triggering very shortly after the end of the timing pulse. If fast resetting was not required, R5, CR3, and CR4 could be deleted, so that both charging and discharging would occur through R4. Or if it is known that V_{in} will not fall back below +1 volt for a long time, T + t must be made larger than this time, by having a large value for R5.

This, of course, is one of the limitations of this circuit, whereas a cascade of the circuits of Figs. 1 and 2 will not have any problem here. Still, this limitation will not be serious or vexing in many applications, as this engineer agreed.

The QFT-5 was chosen for this application for several reasons: its recovery-from-overload time is fairly fast, approximately 1/2 millisecond (whereas the SQ-10a,

PP55AU, etc., are ten times slower and would interfere with accurate, stable timing). And the QFT-5's input currents remain low and input impedances high even if overdriven with ±5 volts of differential overdrive (which a Q-101 or T52 will not, as their input-protection circuits will cause low differential input impedance when overdriven). And the QFT-5's low I_B would permit the use of many megohms for R4, R5, as needed. But for fast work, the T82AH, Q85AH, or Q25AH would be good. The 4.3kΩ/3.3kΩ/1kΩ network at the output was chosen to convert a ±12 volt output swing into a +5 volt, −0 volt excursion, suitable for driving the monolithic gates that were the load.

Of course, operational amplifiers were originally designed to activate and impart precision to analog feedback loops. Operational amplifiers have been developed to such a high degree, however, especially in terms of high gain, low input current and voltage offsets and drifts, fast response, compact size, and low cost, that they are a (pardon the expression) logical choice for many applications where a high-precision open-loop sensing (or crossing-detector) amplifier is required.

The Model QFT-5 which we recommend here provides adequate accuracy and precision of application. To provide greatly improved accuracy (which was not required), we would easily recommend active sensing and timing circuits which would, alas, take three or more operational amplifiers – an unwarranted expense.

Admittedly, a good designer could design a low-drift Schmidt trigger and a temperature-compensated monostable multivibrator using not many more than 10 or 20 transistors, but the extra engineering time and assembly

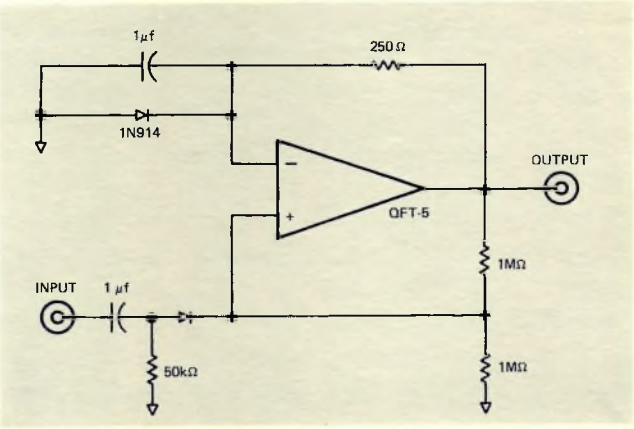


Fig. 1. Monostable Multivibrator Circuit, Borrowed from Philbrick/Nexus Applications Manual, Section II.41

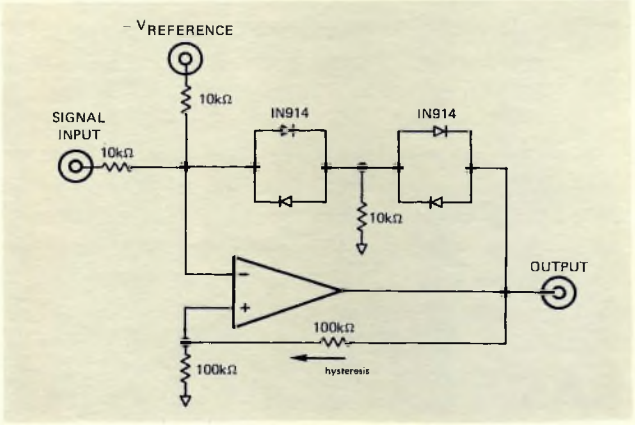


Fig. 2. Comparator or Crossing Detector Circuit, Borrowed from Philbrick/Nexus Applications Manual, Section III.21

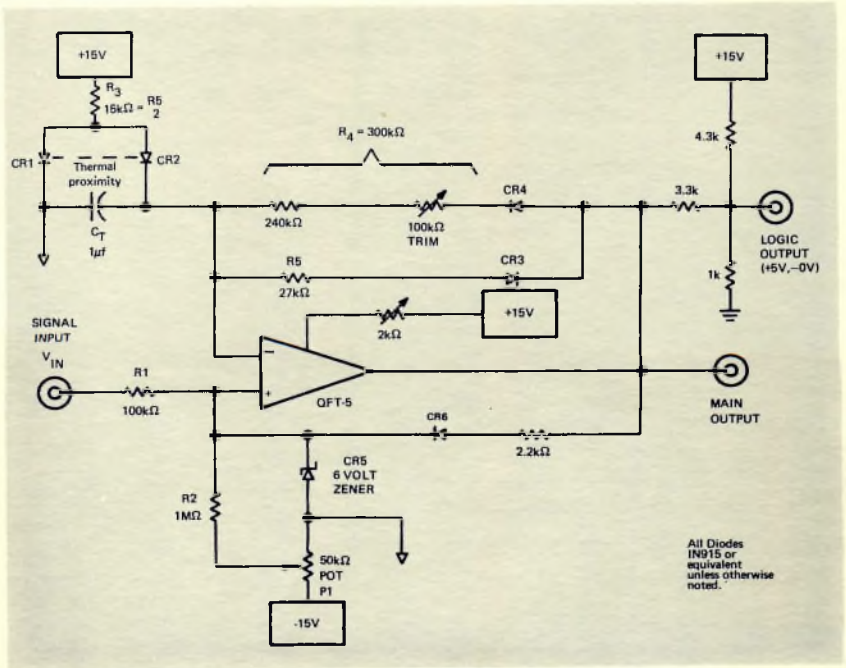


Fig. 3. Combination Crossing Detector and Monostable Multivibrator.

labor in production would make such an approach a doutful economy. Is it not far better if you can buy, off the shelf, at modest cost, a single active element to do all the work?

This circuit will probably not turn out to be an all-time favorite, or solve problems for very many people, but we include it here because it demonstrates that we know how to make our amplifiers hold down two jobs, and accomplish two tasks for the price of one. Applications where an amplifier "wears two or even three hats" are certainly not limited to switching circuits. We have successfully handled similar problems involving multiple duties of the same amplifier in linear and quasi-linear applications, where the loop remained permanently closed.

THE GENERATION GAP
(a hybrid circuits status report)

G.T. Lee, M.S.E.E.

Philbrick/Nexus has combined the best aspects of monolithic and discrete device technologies to create the "now" generation of the operational amplifiers—the hybrids. They embody all of the desirable characteristics of the discrete – component amplifiers, including ease of application, excellent electrical performance and freedom from the necessity to provide external supporting components. At the same time they offer increased mechanical ruggedness, higher reliability, size reduction and cost savings approaching that of their monolithic counterparts without compromising the performance characteristics inherent in the single silicon block approach.

The Philbrick/Nexus amplifiers are usually provided in any one of three standard packages. These are: (1) the low-profile 12 lead TO-8 case, (2) hybrid dual-in-line package (mechanically interchangeable with the monolithic DIP), and (3) the minicube (0.6" square by 0.2" high). These can usually be supplied as hermetically sealed or plastic encapsulated packages – the latter generally resulting in a lower cost.

The hybrid amplifier truly offers a third choice between the discrete and monolithic circuits. We recommend its use in many stringent applications previously requiring the use of discrete modules and in special circuits where the limited quantity (usually less than 50,000) of amplifiers does not warrant the large tooling charges and long delays associated with producing nonstandard monolithic devices. The introduction of this new family of operational amplifiers is the culmination of a strong effort to establish industry's strongest capability to design, evaluate and build linear hybrid circuits. The choice of products was made after an exhaustive market research effort to determine the majority of our customer requirements. The circuit design was performed by our engineering department whose creative new product development work has allowed us to become industry's largest supplier of discrete component operational amplifiers. Special test systems and production methods have been developed to evaluate, match over a temperature range, and assemble individual chip components. In order to obtain complete versatility, we have established the capability of producing both thick-film and thin-film resistors on a variety of substrate materials. The full resources of our application and engineering departments are available to help our customers with their analog problems. Our engineers are in an excellent position to recommend the right hybrid amplifier for the job or to suggest a discrete or monolithic device if one of the two latter approaches presents a better solution.

The present line of hybrid circuits consists of eleven new products and two previously available (and now very popular), amplifiers (Q25AH and Q85AH). The devices have been judiciously selected to cover the broadest possible spectrum of usage from micro-power to high speed and from high reliability to low cost. The table at the end of this article shows their electrical characteristics. A brief description of each type is given below.

Micro-Power (1402 Series and 1404 Series)

The Philbrick/Nexus types **1402, 1402/01** and **1402/02** are FET input, thin-film hybrid operational amplifiers designed to meet the needs of high input impedance ($10^{12}\Omega$), low bias current (5 pA), and low quiescent power (500 μA). These units can be operated over a wide range of supply voltages (±4V to ±24V) and can provide output voltages to within 1 volt of the supply. They are internally trimmed with guaranteed offset as low as 300 μV and have a minimum slew rate of 3 volts per microsecond. Even though the units operate on low quiescent power, they can provide output currents of 5 mA typically with a ±2 mA output guaranteed. As on all of our general-purpose hybrids, they are internally compensated, have a 6 db per octave roll-off, and are unconditionally stable even with large capacitive loads. The 1402 series is encased in a hermetically sealed low-profile TO-8 can to match modern demands for a versatile FET amplifier with minimum dimensions, and offering superior isolation and guarding of the input terminals.

The **1404, 1404/01** hybrid operational amplifiers are specifically designed for low quiescent power applications and are ideally suited for long-term battery operation. These units offer excellent performance with power supply voltage varying from ±2 volts to ±18 volts. The no-load current drain is 60 microamperes, giving a low quiescent power of 250 microwatts. Even with this low power drain at no-signal conditions, the 1404, 1404/01 will deliver up to 4 milliamperes of output current. Because of the unique design of the demand-output-stage, crossover distortion is minimized while the output, which is short-circuit-proof,

will swing nearly to ± supply voltage. Another useful feature of the 1404 series is its internal 6 db per octave roll-off phase compensation which allows stable operation down to unity closed-loop gain configurations without addition of external components. With a small-signal unity gain frequency of 100 kHz, a full output frequency of 10 kHz is obtained.

The **1404, 1404/01** are packaged in the hybrid DIP compatible with the 709 dual-in-line pin configuration which allows adjacent units to be mounted on 1/2 inch centers. The physical construction includes a thin-film and a thick-film complex array in order to obtain a wide range of resistor values required by the amplifier design. Specially-matched transistor chips mounted on the ceramic substrate complete the fabrication.

Low offset current (2 nA @ 25°C and 4 nA @ -25°C), low bias currents (15 nA), low initial E_{os} (1 mV), low offset voltage temperature coefficients = (10 μV/°C), and high CMRR (100 db) are input characteristics which make this series especially attractive for high-accuracy applications.

Hi-Rel Devices (Q25AH, Q85AH)

Philbrick/Nexus **Q25AH** is a wideband, high-reliability, FET-input amplifier. This unit was designed to operate over the full military temperature range (-55°C to +125°C). Its reliability is unquestionable since over one million hours have now been logged on this device and no failures have occurred. Voltage drifts during the million hours have all been smaller than 1 millivolt per year. It provides a combination of outstanding performance such as high speed (30 MHz gain-bandwidth), very high input impedance (10^{12} ohms), low bias current (50 pA), good common-mode performance (10,000), and low noise (2 μ V for a bandwidth of 160 Hz to 16,000 Hz), and is virtually immune to external circuit or signal stress: shorts, overloads, over-voltage, excessive inputs, and other abnormal external conditions. The complete amplifier is enclosed in a low-profile TO-8 transistor case. Its components and construction are of the highest quality – all silicon semiconductors, conservatively rated circuit elements, and hermetic-sealing in an isolated metal case (permitting driven guard connection).

The Philbrick/Nexus **Q85AH**, like the **Q25AH**, is a hybrid differential operational amplifier, designed to meet the stringent requirements of high reliability applications. The unit is also packaged in a hermetically-sealed low-profile TO-8 case and has the same pin connections as the Q25AH. This unit will do an exceptional job for applications where the high input impedance of the Q25AH is not needed. It, too, has high gain-bandwidth product (30 MHz minimum), very good common-mode rejection (30,000), and low noise (2 μV rms maximum, 160 Hz to 16,000 Hz). The input impedance is 2 megohms and the device has a guaranteed output of ±11V, ±2.2 mA over the full military temperature range (-55°C to +125°C).

Lifetest results to date show no failures in 1.8 million hours logged.

Economy Devices (1406, 1407 Series, 1408 Series)

The **1406** hybrid operational amplifier has been designed as a general purpose amplifier, priced well below FET-input hybrids, yet it exhibits many of the best characteristics of the higher priced units. It has full output power to 75 kHz, (at V_o = ±10V and I_{out} = ±5 mA), open-loop gain of 50,000 and a unity gain bandwidth of 2 MHz. Good common-mode characteristics with a common-mode range of ± 11 V, a CMRR of 100,000 and the ability to withstand large differential input voltages (±30V), make it ideal for comparator applications. In addition, the 1406 features fast slew rate and fast settling time.

This operational amplifier is self-sustained with no external compensation or balance trimming required, and is stable for all feedback configurations. The amplifier is packaged in a low-profile TO-8 case of all-metal construction and combines the latest in thick-film and monolithic technologies to provide maximum reliability and performance. Last, but not least, it operates from supply voltages between ±5V and ±20V at the low quiescent current of 2 mA.

The **1407** and **1407/01** are new high-speed, high-performance FET hybrid amplifiers offering the utmost in performance over the commercial temperature range (-25°C to +85°C). Many of the same high-quality features offered by the Q25AH can be found here. High input impedance ($10^{11}\Omega$), wide gain-bandwidth product (30 MHz), and fast slew rate (8 V per μsec minimum) make these units ideal for comparator, integrator, and sample-and-hold applications. They provide modest output capability (±11V, ±2.2 mA) with excellent common-mode characteristics (common-mode range of ±10V with rejection ratio of 10,000). These units, encased in the low-profile TO-8 package, can be utilized wherever good reliability, small size, high input impedance, and good speed are required.

New members, the **1408, 1408/01** and **1408/02**, join the Philbrick/Nexus family of hybrid operational amplifiers. They are high-gain wide-bandwidth hybrids available in a minicube package. FET-inputs and thick-film construction have been combined to achieve full-power output response (±10 V, ±5 mA) of 125 kHz, with a respectable unity-gain bandwidth of better than 3 MHz. High CMRR has also been maintained, typically 80 db. Superior input characteristics qualify the 1408 series for a myriad of applications. They function ideally as accurate voltage followers, integrators, track-and-hold amplifiers, plus a host of other operations where high impedance, low dc input current devices are

mandatory. Both differential and common-mode impedances are high (10^{11} ohms) while input bias current is as low as 5 pA. Open-loop gain is an impressive 500,000; high dynamic transfer accuracies are therefore attained with ease. The 1408 series requires no external trimming or compensation and input voltage offset of 1 mV with a temperature coefficient of 25 μV/°C is obtained. The series consists of truly outstanding performers considering their low price and uncompromised quality. The speed and accuracy designed into these amplifiers qualify them to be in contention with, and in many cases to surpass, more expensive discrete offerings.

The following table gives the electrical characteristics of the presently available Philbrick/Nexus hybrid amplifiers.

CHARACTERISTICS Typical at 25°C, Nominal power supply, unless indicated otherwise	Q25AH	Q85AH	1402/01/02	1404/01	1406	1407/01	1408/01/02
Symbol **OUTPUT RANGE**							
E_o Voltage ..... min	±11V	±11V	+ | Vcc-2 | V	±|Vcc-3|V	±10V	±11V	±10V
I_o Current ..... min	±2.2mA	±2.2mA	±2mA	±1mA	±5mA	±2.2mA	±5mA
VOLTAGE GAIN (DC, open loop)							
A_o Rated load ..... min	20,000	20,000	10,000*	25,000	10,000	20,000	25,000
10K load ..... min	40,000	40,000	– –	– –	20,000	40,000	100,000
FREQUENCY RESPONSE (inverting)							
f_t Small signal (unity gain, open loop) ..... min	30MHz*	30MHz*	1.0MHz	0.1MHz	1MHz	30MHz*	4MHz (typ)
f_s Large signal: full output (undistorted) .... min	100kHz	100kHz	70kHz	5kHz	50kHz (typ)	100kHz	—
f_p full output (peak to peak) .. min	167kHz	167kHz	– –	8kHz	90kHz (typ)	200kHz (typ)	70kHz
sr Rate limit	8V/μ Sec	8V/μ Sec	3V/μ Sec (min)	0.3V/μ Sec	5V/μ Sec	8V/μSec	3V/μ Sec(min)
t_s Settling time (0.1%)	– –	– –	– –	50μSec	9μSec	17μ Sec	– –
INPUT VOLTAGE RANGE							
E_{cm} Common mode (DC linear operation) .... min	±10V	±11V	+ | Vcc-3 | V	±|Vcc-4|V	±10V	±10V	±10V
(fault) ..... abs max	+15V	±15V	±Vcc	±Vcc	±15V	±15V	+15V
E_{diff} Differential (between inputs) ..... abs max	30V	20V	2Vcc	2Vcc	30V	30V	30V
CMRR Common Mode Rejection Ratio (DC) .	5000 (min)	20,000 (min)	6500	50,000	100,000	10,000	10,000
INPUT VOLTAGE OFFSET							
E_{os} Initial (without external trim) @ 25°C	10mV(max)	10mV(max)	+3/1/0.3mV	±5/1mV	±2mV	±10mV(max)	±2/1/1mV
Zero adjustment	250kΩpot.(optional)	250kΩpot.(optional)	1kΩpot.(optional)	1MΩpot.	internal trim	250kΩ(optional)	internal trim
E_{os} TC Vs. temperature (avg, -25°C to +85°C) .. max	±55μ V/°C	±27μ V/° C	+50/30/10μ V/°C	±20/10μ V/°C	±30μ V/°C	±55/25μ V/°C	±75/25/25μ V/° C
$\Delta E_{os}/\Delta t$ Versus time (per day)	±50μ V	+50μ V	±25μ V	±50μ V	±50μ V	±50μ V	±50μ V
PSRR Versus power supply	70μ V/V	25μ V/V	400μ V/V	50μ V/V	35μ V/V	70μ V/V	350μ V/V
INPUT BIAS CURRENT							
I_{bias} Initial @ 25°C ..... max	–150pA	+220nA	–30pA	+30nA	+1μ A	–150pA	–25/10/5pA
$\pm I_{bias}$ TC Vs. Temperature (avg, -25°C to +85°C) .. max	15pA/°C**	4nA/°C	3pA/°C	0.5nA/°C	9nA/°C	15pA/°C**	2.5/1/0.5pA/°C*
$\Delta I_{bias}/\Delta V_{cc}$ Vs. power supply	10pA/V	5nA/V	3pA/V	350pA/V	20nA/V	10pA/V	3pA/V
$\Delta I_{bias}/\Delta t$ Vs. time (per day)	±3pA	±5nA	±1pA	– –	– –	±3pA	±1pA
I_{diff} Difference (tracking).	10pA	10nA	10pA	7nA	75nA	10pA	10/5/2pA
INPUT IMPEDANCE							
Z_d Differential	10^{11} Ω‖ 3pF	2M Ω‖ 3pF	10^{12} Ω‖ 4pF	4MΩ‖ 10pF	300kΩ‖ 3pF	10^{11} Ω‖ 3pF	10^{11} Ω‖ 4pF
Z_{cm} Common mode (either input to common) .	10^{12} Ω ‖ 6pF	500M Ω‖ 5pF	10^{12} Ω‖ 10pF	1000MΩ ‖ 10pF	300M Ω‖ 4pF	10^{12} Ω‖ 6pF	10^{11} Ω‖ 4pF
NOISE (Referred to input)							
Flicker (0.016 to 1.6Hz)							
e_n Voltage p-p.	5μ V	5μ V	6μ V	6μ V	5μ V	6μ V	6μ V
i_n Current p-p	0.2pA	200pA	0.1pA	100pA	200pA	0.2pA	0.2pA
Midband (1.6 to 160 Hz)							
e_n Voltage rms	2μ V	1μ V	2μ V	1μ V	2μ V	2μ V	2μ V
i_n Current rms	1pA	30pA	1pA	60pA	100pA	1pA	1 pA
Broadband (160 Hz to 16kHz)							
e_n Voltage rms	2μ V	0.8μ V	2μ V	2μ V	2μ V	2μ V	2μ V
i_n Current rms	3pA	30pA	2pA	50pA	100pA	3pA	3pA
POWER REQUIREMENTS							
$\pm V_{cc}$ Nominal supply voltage	±15V	±15V	±15V†	±4.5V*	±15V	±15V	±15V
Voltage range	+12 to ±18V	±8 to ±18V	±4 to ±24V	±2 to ±18V	±14V to ±16V	±12 to ±18V	+10V to +22V
I_{cc} Current: quiescent ..... max	±7.6mA	±7mA	±1.0mA	±75μ A	±7mA	±7.6mA	±9mA
full load ..... max	9.8mA	9mA	3.0mA	1.2mA	12mA	9.8mA	14mA
TEMPERATURE RANGE (degrees C)							
Operating	-55 to +125	-55 to +125	-25 to +85	-25 to +85	-25 to +85	-55 to +125	-25 to +85
Storage	-62 to +150	-62 to +150	-55 to +125	-55 to +125	-55 to +125	-62 to +150	-55 to +125
OUTLINE DRAWING	TO-8	TO-8	TO-8	S-2 (D.I.P.)	TO-8	TO-8	T-1
SOCKET	US-Q ($3.50)	US-Q ($3.50)	US-Q ($3.50)	—	US-Q ($3.50)	US-Q ($3.50)	6035 ($2.50)
PRICE (1-9)	$180	$161	$75/95/115	$58/65	$26	$63/70	$30/33/35
SIMILAR MODELS	—	—		1006	Q-200	Q25AH, hi-rel Mil version	—
	*@ gain of 100 see data sheet **@ 25°C, doubles each 10°C, I_b = 10nA(max) @ +85°C	* @gain of 100 see data sheet	*@ 7kΩ load **@ 25°C, doubles each 10°C, I_b = 2nA(max) @ +85°C †Universal Power Supply Range	*Universal Power Supply Range		* @ gain of 100, see data sheet **@ 25°C, doubles each 10°C, I_b = 10nA(max) @ +85°C	*@ 25°C, doubles each 10°C, I_b = 1/0.5/0.25 nA(max)@ +85°C

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