STABILIZATION OF WIDE-BAND DIRECT-CURRENT AMPLIFIERS FOR ZERO AND GAIN*

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Summary—*A method for automatically stabilizing direct-current amplifiers against zero offset voltage and voltage drift is described. Stabilization is obtained through the application of a mechanical chopper to detect any zero offset error voltage. The circuit is such that the stabilization device does not alter the high-frequency response characteristics of the amplifier. Primary application has been in the field of analogue electronic computers.*

A MAJOR OBSTACLE in the application of direct-current (dc) amplifiers has been their inherent dc voltage offset and drift which, in general, has been compensated by means of manual adjustments. This difficulty has been overcome for the case of narrow band amplifiers by utilizing a mechanical chopper to change the dc voltage into an alternating-current (ac) voltage, amplifying the resultant with an ac coupled amplifier, and rectifying the output of the ac amplifier.[1] The available bandwidth of such a system is a function of the frequency of the mechanical chopper. This paper will describe an amplifier which utilizes a mechanical chopper for stabilizing with respect to dc without affecting the high frequency response.

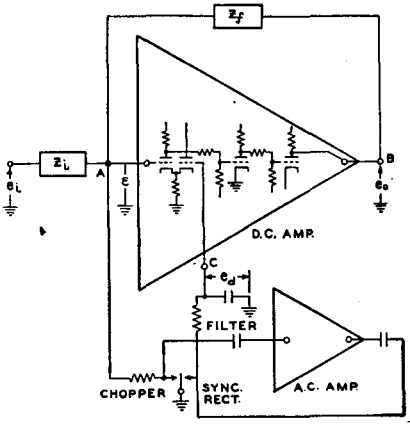

Fig. 1—Basic diagram of the stabilized dc amplifier.

Figure 1 is a block diagram of one form of the stabilized amplifier. It consists of a normal dc coupled feedback amplifier plus a mechanical chopper, an ac coupled amplifier, and a synchronous rectifier. The chopper samples the potential which appears at the summing point, *A*.

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[1] A. J. Williams, Jr., R. E. Tarpley and W. R. Clark, "D-C Amplifier Stabilized for Zero Gain," *A.I.E.E. Transactions*, Vol. 67, pp. 47-57, 1948.

This voltage is amplified and rectified, and the output voltage of the rectifier is applied to the amplifier at some point, C, where a zero setting voltage may be inserted provided this point is not the summing point A. The rectifier is provided with a long time constant filter in order that components of the chopper frequency will not appear on the output of the dc amplifier. The input to the chopper is provided with a filter for reducing error voltage components of chopper frequency in order that ac input voltages synchronous with chopper frequency will not cause a dc voltage to be developed by the synchronous rectifier which would cause the dc amplifier to have a dc offset.

The operation principle of the amplifier may best be understood from the following mathematical analysis. Assume that the internal gain of the dc amplifier is equal in magnitude for signals inserted either at point A, the summing point, or at point C, the place where the zero set voltage is normally applied.

Let $G_1(\omega)$ = Gain of dc amplifier.

$G_2(\omega)$ = Gain of chopper, amplifier, rectifier chain.

k = Zero set voltage which would normally be necessary to cause e_o to be zero when ϵ is zero. This is the normal offset voltage of the amplifier referred to the input.

e_i = Input voltage to amplifier.

e_o = Output voltage of amplifier.

ϵ = Voltage at summing point.

e_d = Voltage at zero set point.

Z_i = Input impedance.

Z_f = Feedback impedance.

$$e_o = (\epsilon - e_d + k)\,G_1(\omega) \tag{1}$$

$$e_d = \epsilon G_2(\omega) \quad \text{(Note that } e_d = 0 \text{ when } \epsilon = 0. \text{ The chopper insures this for dc)} \tag{2}$$

$$\frac{e_i - \epsilon}{Z_i} = \frac{\epsilon - e_o}{Z_f} \tag{3}$$

$$\epsilon = \frac{Z_f}{Z_f + Z_i}\,e_i + \frac{Z_i}{Z_f + Z_i}\,e_o \tag{4}$$

$$e_d = \frac{Z_f}{Z_f + Z_i} e_i G_2(\omega) + \frac{Z_i}{Z_f + Z_i} e_o G_2(\omega). \tag{5}$$

By eliminating ϵ and e_d in the above equations, the following expression is obtained for the output voltage of the amplifier.

$$e_o = \frac{e_i \left[\frac{Z_f}{Z_f + Z_i} G_1(\omega) - \frac{Z_f}{Z_f + Z_i} G_1(\omega) G_2(\omega) \right] + k G_1(\omega)}{1 - \frac{Z_i}{Z_f + Z_i} G_1(\omega) + \frac{Z_i}{Z_f + Z_i} G_1(\omega) G_2(\omega)}. \tag{6}$$

If $\frac{Z_i}{Z_f + Z_i} G_1(\omega)$ is made very large relative to unity, the unit term in the denominator will have negligible effect and may be omitted. The expression for the output voltage as a function of the input voltage may then be written:

$$e_o = - e_i \frac{Z_f}{Z_i} + k \frac{Z_f + Z_i}{Z_i \{G_2(\omega) - 1\}}. \tag{7}$$

The first term on the right-hand side is desired, and the second term is the zero offset voltage term. Note that in order to reduce the zero offset voltage, it is only necessary to make $G_2(\omega)$ large at dc. $G_2(\omega)$ may be made large enough so that the second term of (7) is negligible, in which case the gain is

$$e_o = - e_i \frac{Z_f}{Z_i} \tag{8}$$

which states that the gain is the ratio of the feedback impedance to the input impedance, and that there is no dc offset.

The zero stabilizing circuit not only eliminates the zero and drift problems common to dc amplifiers, but also effectively increases the loop gain. The expression for the loop gain is

$$\mu\beta = \frac{Z_i}{Z_f + Z_i} \{G_1(\omega) - G_1(\omega) G_2(\omega)\}.$$

At zero frequency, $G_1(0)$ and $G_2(0)$ have opposite signs, and the magnitude of the loop gain is enhanced by the factor $G_2(0)$ very nearly. At high frequencies, $G_2(\omega)$ becomes very small, so the stabilizing circuit has little effect on the loop gain at high frequencies.

Practical Amplifier

The schematic diagram of an amplifier using this principle is shown in Figure 2. The dc amplifier contains a 5692, a 6SH7, and a 6V6 tube. Phase control networks are included to insure stable operation for a wide variety of input and feedback networks. The stabilizer utilizes a 386-cycle chopper and two type 5693 tubes. The chopper is

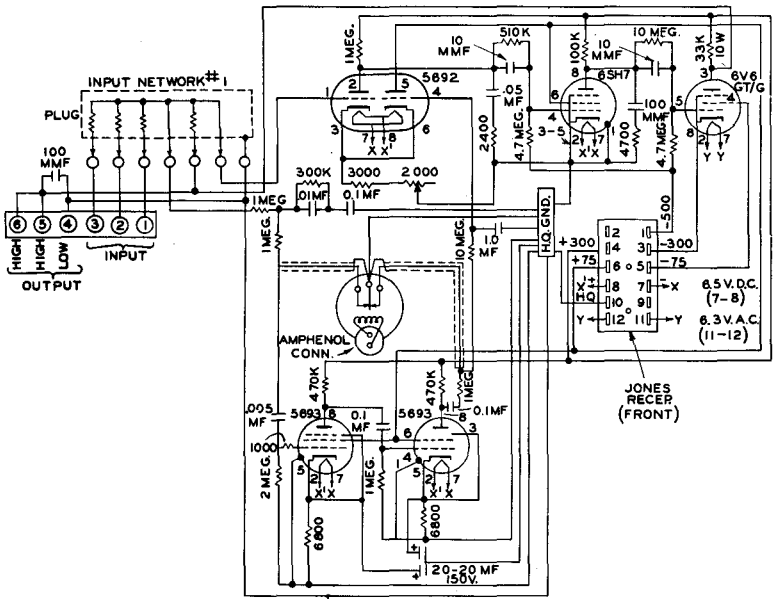

Fig. 2—Schematic diagram of a typical stabilized dc amplifier.

driven from a 193-cycle source and operates at double this frequency since it is unpolarized, i.e., contains no permanent magnet. This mode of operation minimizes the possibility of a dc offset occurring due to stray pick up of the chopper drive signal into the ac amplifier. Synchronous rectification is obtained from a pair of contacts on the chopper. These contacts are well shielded in order that no oscillation of the ac amplifier will be caused by stray coupling between them. The same net effect can be obtained by adjusting the contacts to overlap in order that one or the other will be grounded at all times. Gain of the dc amplifier is around 50,000 and gain of the stabilizer is about 3000 for zero frequency resulting in a total gain of about 150,000,000.

When Z_f and Z_i are equal (gain of unity), the feedback factor is 75,000,000, which is quite high. At dc, this amplifier is capable of producing a swing from —200 volts to +200 volts across a load resistance of 100,000 ohms.

The frequency response of this amplifier depends on the input and feedback networks. When these networks are identical (say equal resistances) the amplifier has a gain of unity and is flat at least out to 100 kilocycles. This amplifier was developed specifically for application in electronic analogue computers, and may be used as a summing amplifier, integrator, or differentiator, dependent on the input and feedback networks used. Figure 3 shows how the amplifier is adapted for these specific applications. The stabilizer makes the frequent manual zero adjustment of dc computer amplifiers entirely unnecessary, and holds the offset to a much lower value than can ever be done practically through manual adjustments. When used for the integrator application, the drift rate is extremely small, and when used as a summing amplifier or differentiator the spurious dc offset is held to a very low value. In the actual amplifiers constructed, the offset is generally less than 50 microvolts referred to the input when the input and feedback networks have impedances in the megohm range. The small offsets encountered are due to (1) spurious potentials developed within the chopper itself due to contact potential, thermals, etc., (2) grid current in the first stage of the dc amplifier (which would cause an output voltage of $Z_f \times$ grid current, (3) lack of infinite gain in the ac amplifier. Item (3) would cause an offset referred to the input of $\frac{e_{do}}{G_2(0)}$ to first approximation where e_{do} is the voltage normally required at point C to zero the amplifier. Should the resulting small offset from these causes be greater than desired for some particular application, it could of course be reduced by a manual zero adjustment.

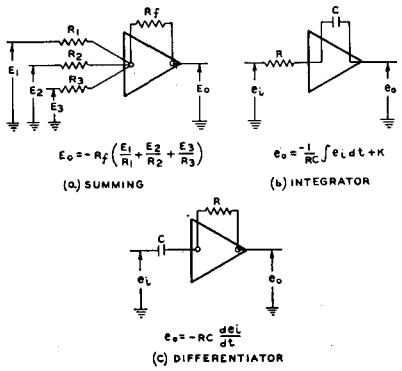

Fig. 3—Diagrams illustrating several basic computer applications for the dc amplifier.