Current-steering chip upgrades performance of d-a converter

AN-17

Steered bit-switching currents produced by a dielectrically isolated monolithic IC provide increased speed and accuracy by avoiding thermal tails, the lag in time involved in stabilizing switching transistors

by Ed Maddox, *Teledyne Philbrick, Dedham, Mass.*

☐ Improvements in the operation of precision digital-to-analog converters have been brought about primarily by improvements in the bit switches. These are binarily weighted switchable current sources that sum their currents in a resistor to generate voltages that correspond to the digital inputs. There is one bit switch for each digital input to the converter, and each must switch a current on and off in response to a digital command at the input.

One of the major problems in obtaining high precision and speed in d-a converters has been the thermal settling time involved in turning the current-source transistors on and off. This and other problems have been solved by current steering. This technique is employed by Philbrick's monolithic pnp bit switch, which will soon be available to OEM users.

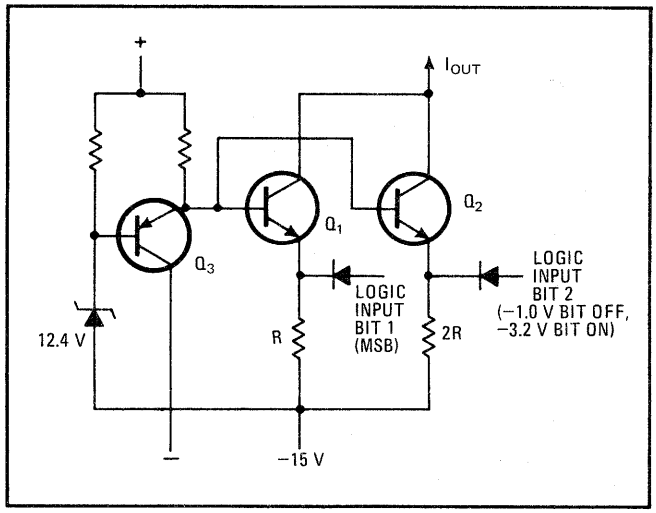
Current steering is a method by which the current-source transistors operate continuously while the current to the output is switched by an auxiliary transistor. Current steering is not new—it has been used in discrete-component circuits. But when such a circuit is built in monolithic integrated-circuit form, it produces significant improvements in the converter's speed and thermal performance.

The new monolithic array of bit switches uses dielectrically isolated pnp transistors in the current-steering mode. The transistors are configured to avoid the effects of thermal gradients on the chip, while a low output capacitance permits better rise times than have been possible in the past. And, because the transistors are built in a monolithic circuit, it is economical to use current-sharing methods to equalize base-emitter voltages, thereby reducing errors.

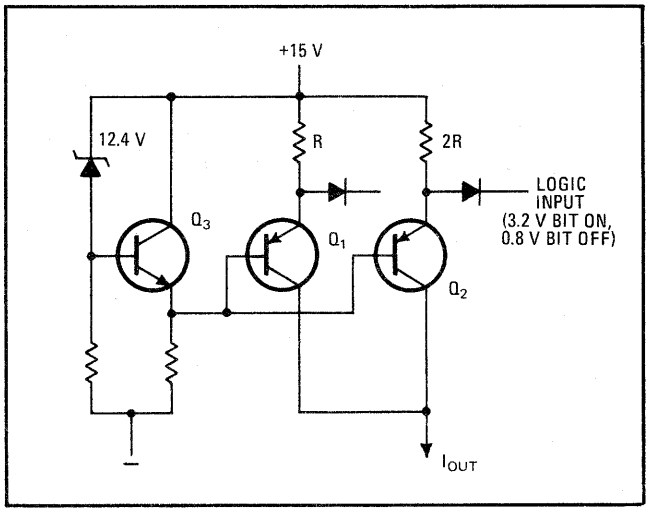
This bit switch, in achieving its basic objective of switching bit currents without degrading the speed or accuracy of the d-a converter, also meets these desirable criteria over the entire temperature range:

- Provides TTL-compatible interfacing (on voltage is 2.0 V, and off voltage is 0.8 V).
- Responds quickly to digital commands.
- Is accurate enough for use in high-resolution d-a converters.

Accuracy can be separated into two factors—linearity and scale-factor accuracy. Linearity is the degree to which the ratios between the values of individual bits are set and maintained. Scale-factor accuracy is the degree to which the converter produces the desired output



1. Diode-npn switches. Transistors Q_1 and Q_2 are switchable current sources whose currents are set by resistors R and 2R. Q_3 transfers 12.4-V zener drop to resistors R and 2R to help set the individual currents. Output current I_{OUT} goes to a summing resistor. Unequal heating or cooling can cause imbalances in the base-emitter voltages of the transistors and also in the current gains, both of which affect accuracy. Logic inputs were not compatible with TTL levels.



2. Diode-pnp. Nearly a mirror image of the circuit in Fig. 1, this circuit provides compatibility with TTL-logic inputs, but it still shows the same deficiencies in compensating for changes in transistor-current gains and base-emitter voltages.

magnitude. For example, a converter could have good linearity, but poor scale-factor accuracy; this condition may be acceptable in certain applications.

Evolution of bit switches

Tracing the development of bit switches over the past five years or so sheds a great deal of light on improvements that have evolved. The characteristics of five major previous types of bit switches, as well as the new switch, are summarized in the table, p. 129.

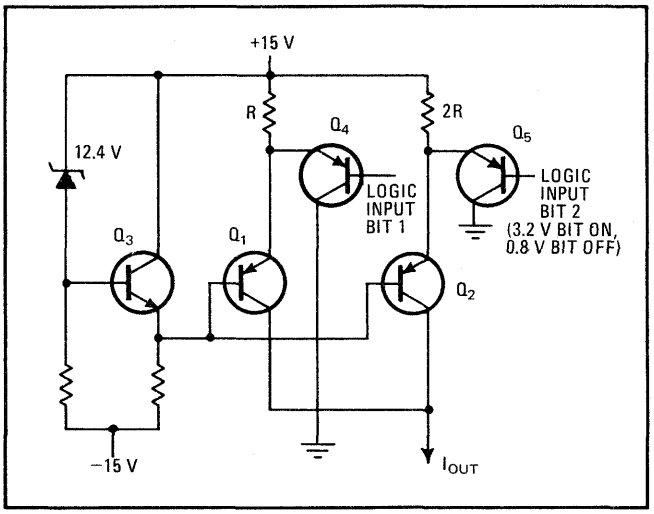
■ *The discrete diode-npn switch* was one of the earliest forms of current-switching bit switches. It used discrete npn transistors to switch the current sources. In Fig. 1, transistor Q_1 and resistor R form one current source, and Q_2 and 2R form another that has half the current value of the first. The 12.4-v reference zener sets Q_3's base at about (−15 + 12.4 v), or about −2.6 v.

The base-emitter voltage (V_{BE}) of Q_3 approximately cancels the V_{BE} of Q_1 and Q_2, and thus the voltages across R and 2R are about equal to the voltage across the 12.4-v zener. A diode couples the logic signal to the transistor emitter and when the logic is at its high level (−1.0 v), the transistor is biased off, and no current is fed to the output. When the logic input is low (−3.2 v), the diode is biased off, the transistor turns on, and the resistor current is fed to the output.

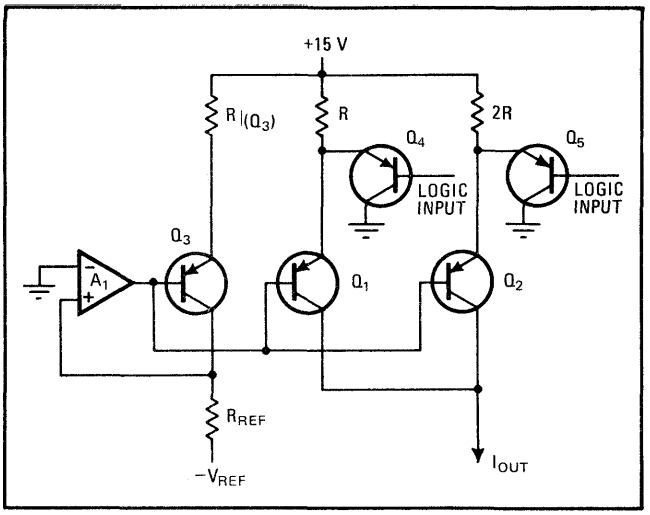
This circuit's speed is affected by the coupling diode's recovery time and the finite time constant for a voltage change at the Q_1 or Q_2 emitter, which also reduces switching and settling speed. Any difference in switching speed from one transistor to another causes glitches in the converter output.

Thermal problems are substantial, too. A difference in the V_{BE}s of Q_1 and Q_2 results in unequal voltages across R and 2R and thus an error in the bit ratio, affecting linearity. Although this difference could be initially canceled by trimming the values of R and 2R, unequal heating or cooling of Q_1 and Q_2 could cause subsequent differences in the V_{BE}s, and that difference produces errors in bit ratio.

When the logic command turns on a transistor, there is a change in transistor dissipation, and the final bit value will not be reached until the transistor stabilizes thermally. The primary mechanism involved here is the variation of V_{BE} with temperature. A discrete-component assembly usually has long thermal time constants and poor thermal coupling between bit switches, producing a long final settling time, commonly referred to as a thermal tail.



3. Pnp-pnp. Replacing diodes of Fig. 2 with transistors eliminates diode storage times and thus raises speed, but this change does not affect problems of changing current gain and base-emitter voltages.



4. Adding a reference servo. Addition of an operational amplifier helps to compensate for changing current gain and base-emitter voltage. All bases are adjusted to maintain constant current through Q_3, and, if the transistors are matched, the currents through Q_1 and Q_2 are thus controlled by the operational amplifier.

The npn-diode circuit of Fig. 1 has no compensation for variations in α (current gain) that result from temperature changes in Q_1 and Q_2. The zener reference voltage, repeated across R and 2R, establishes specific currents through R and 2R, but these are transistor-emitter currents. Since α is less then 1 (finite I_{base}) and subject to change with transistor temperature, the Q_1 and Q_2 collector currents (which make up the output current I_{out}) will change with operating temperature. If Q_1 and Q_2 change α in a matched or tracking fashion, the ratio of bit values may not err, but the scale factor will show an error. The V_{BE}s of Q_1 and Q_2 (npns) are essentially compensated by the opposite V_{BE} of Q_3 (pnp). This is effective, but crude, since the pnp and npn devices never match well. Also, a current leakage through the coupling diode of a turned-on bit could produce significant error at elevated temperature, which usually limits resolution to less than 12 bits.

One final limitation of this circuit is its sensitivity to power-supply voltage variations. As the supply voltage shifts, the logic threshold likewise shifts.

■ *The diode-pnp circuit* of Fig. 2, a logical variation of the circuit of Fig. 1, is the basis for many converters. It produces a direct DTL/TTL-compatible logic input (with a slight bending of standards for TTL-logic high), deleting one shortcoming of Fig. 1. Otherwise its problems are very similar to the diode-npn circuit. And in this circuit, too, the logic threshold level is sensitive to power-supply variations.

■ *The pnp-pnp configuration* in Fig. 3 moves a step ahead by replacing the coupling diode with a transistor, thus removing the problem of diode-storage time and current leakage. The low level of input-logic currents

also improves matters, especially when adapting to other logic levels. The operating speed improves with the elimination of storage-time problems, but many shortcomings remain.

■ *A reference servo* (an operational amplifier) added to the pnp-pnp to compensate for variation in α and V_{BE} was the next advance (Fig. 4). The equivalent job of Q_3—setting the voltage across the bit resistors—in previous circuits is handled here by Q_3 in a quite different circuit arrangement. Q_3 is connected as a current source similar to that in the Q_1 circuit. This current source is sometimes referred to as a dummy bit. Q_3 has in its collector path a resistor (R_{REF}) to which a negative-polarity reference voltage is applied.

An operational amplifier, A_1, drives the transistor bases on a common-voltage bus and adjusts the base voltage so that the Q_3 collector current maintains the A_1 + input terminal at 0 V (the voltage V_{REF} is thus forced across the resistor R_{REF}). If $R_{(Q3)}$—the reference dummy resistor—and R and 2R are matched in ratio, and if Q_1, Q_2, and Q_3 are matched in α, then variations in α are cancelled by the action of the servo loop, consisting of A_1 and Q_3. (If, for example, α decreases, then so do I_C and the voltage across R_{REF}. The op amp then counteracts this change by reducing the base voltage and increasing I_C.) Since the loop regulates I_C for Q_3, a matched set of transistors will produce a stable value of I_C and thus I_{out} for Q_1 and Q_2.

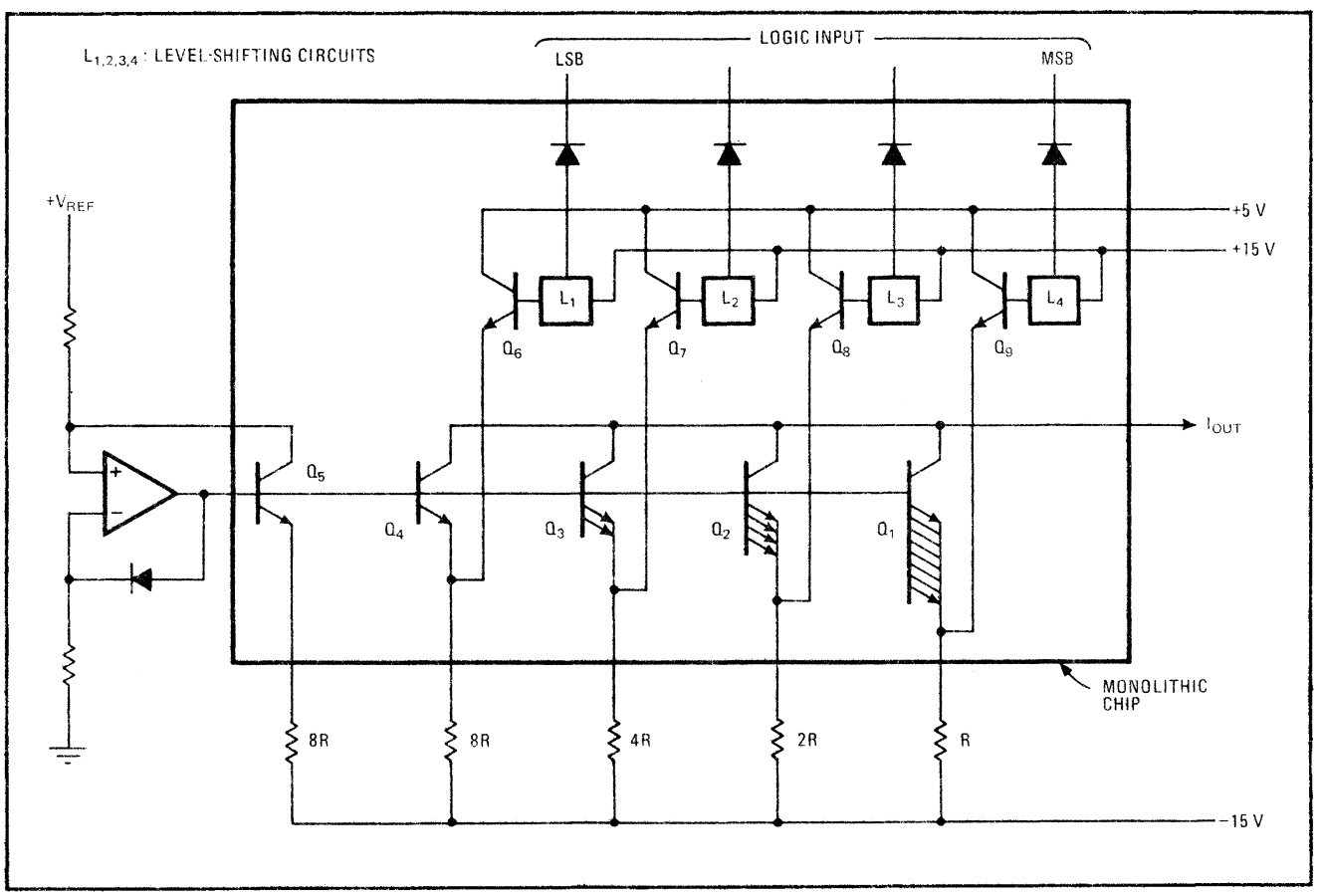
Conveniently, the circuit improvement for compensation also gives a more ideal compensation of V_{BE}, resulting in smaller scaling errors as the temperature changes. The improved compensation is the direct result of using a pnp V_{BE} to match and subtract out a similar pnp V_{BE}. The very best compensation will result when the compensating device (Q_3) is operated at the same I_C as the compensated device (Q_1 or Q_2).

Problems remain

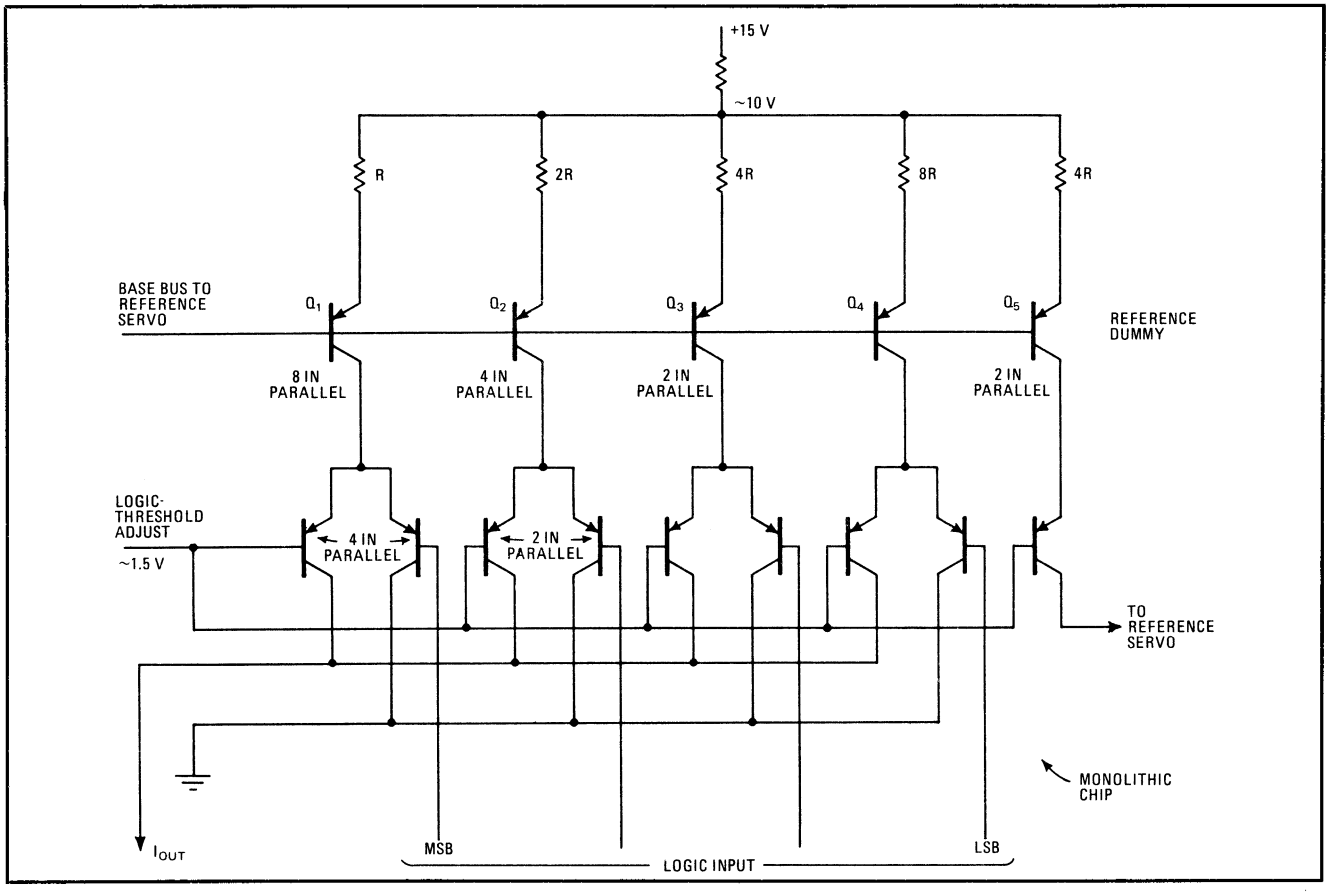
Distinct progress in switching technology was indicated, but problems still remained. The discrete assemblies still had thermal problems associated with the gross distance and poor thermal coupling between devices. Speed was still limited by current-switching times, and the thermal settling tails still persisted. These were perhaps even more noticeable as the improvement in α and V_{BE} compensation made it practical to obtain resolution from 12 to 14 bits, and the tail is thus larger relative to one least significant bit (LSB).

Attempts at higher-resolution designs also brought attention to an additional V_{BE} problem previously ignored here. To achieve ratio tracking, and thus linearity over a wide temperature range, the change in V_{BE} of the individual current-source transistors must track. A matched set of transistors would track, but only if all were operated at the same current.

As the weighting of bit currents for this class of converters is binary for a 4-bit section, each successive bit operates at one half the prior bit's current. Transistors,



5. Monolithic npn. Paralleled transistors in the bit switches assure similar currents through each device and thus similar base-emitter voltages. However, use of npn transistors requires level-shifting circuits (L_{1-4}) to work with TTL inputs. Also, switching is done directly on current-source transistors, which introduces thermal-stabilization problems (thermal tails), as in the discrete-component circuits.



6. Monolithic current-steering. Current-source bit transistors Q_{1-4} operate continuously, while logic inputs switch currents from ground path to output line, thus avoiding thermal tails. Multiple transistors for each bit help assure base-emitter voltage-matching. A reference servo is also used in this circuit; it is not shown to minimize drawing complexity, but is similar to that in circuit of Fig. 5.

when initially matched at equal currents, will operate at a V_{BE} difference of approximately 18 millivolts with a 2:1 current relationship. This difference can be accommodated by changing resistor values, but this will only help at one temperature.

The differential change of V_{BE} with temperature for a transistor pair is approximately 3 microvolts per degree Celsius per millivolt of the V_{BE} difference. Thus an 18-mV initial differential produces a 54-μV/°C tracking error. This error must be considered in relating the voltage appearing across the current-setting resistors R, 2R, and so on, to the differential error in current ratios. Thus, to improve the performance in high-resolution converters beyond the ability of a Fig. 4 circuit, a solution to this V_{BE} tracking problem had to be found.

Monolithic current-sharing helps V_{BE} match

The power of integration was then brought to bear on the problems of the bit switch. Figure 5 illustrates a monolithic npn-based bit switch having four switches with associated level shifters for the logic inputs. This circuit, an available, widely used, standard product, provides the dummy bit for use in a reference-servo circuit to compensate V_{BE} and α.

The problem of differential V_{BE} caused by unequal bit currents is solved by paralleling appropriate numbers of transistors so that all transistors pass equal currents. The monolithic construction results in good matching of the initial values of V_{BE} and α, as well as in thermal coupling not attainable in discrete assemblies. This unit is built with npn transistors to achieve reasonable-quality devices with the standard linear integrated-circuit process.

However, this circuit suffers from other problems. A level-shifting circuit is required. The junction-isolated process produces junction leakage, which limits bit accuracy, especially at elevated temperatures. And bits are switched by turning the current-source transistors on and off, which results in speed problems due to the emitter-circuit time constant and settling problems due to the thermal tail associated with device-dissipation changes.

In this type of bit switch, the geometrical arrangement of the transistors is such that the eight transistors used for bit 1 are arranged in a line. Below, in the same line are the four transistors for bit 2, the two transistors for bit 3, and one transistor for bit 4.

This geometrical arrangement results in problems not evident from the schematic diagram. A thermal gradient across the chip—particularly along the line of transistors—will produce a significant error in V_{BE} matching, which degrades linearity. Such gradients can be generated by external heat sources or internally by heat sources within the chip.

The internal heat sources vary with time because they are dependent on the state of the digital commands. This causes another form of thermal tail, further limiting the high-speed performance of the switch. An addi-

tional problem resulting from the in-line arrangement of the transistors is the mismatches caused by processing diffusion gradients across the wafer. This will reduce the yield for devices usable at high resolution.

Monolithic current steering does it

Philbrick's ultimate goal was to design high-performance d-a and a-d converters. The monolithic pnp quad switch is now being used in the military-grade 4050-series hybrid d-a converters and in display d-a converters. The quad switch (Fig. 6), a 4-bit switch with a dummy bit for the reference servo, is a dielectrically isolated pnp array that provides bit switching by current steering. Paralleled transistors in the current sources permit equal-current operation of the transistors. The use of pnp transistors provides a direct TTL-compatible logic input, thereby avoiding speed degradation and skew associated with logic-level shifting. Further, the logic threshold is programable, offering a flexibility not previously available.

Since, in current steering, the current sources operate continuously, any thermal-tail problems associated with turning current sources on and off are eliminated. The bit currents are turned off and on at the output by the logic-input level turning the logic-input transistor on and off. At logic high, this transistor is off, and the current from the bit-current source is fed through a pass transistor to the output. When the logic transistor is on (logic low), the pass transistor is biased off, and the current flows through the logic transistor to ground.

This current-steering technique aids the dynamic performance of the switch in two ways. First, by eliminating thermal tails through continuous operation of the current sources, the time required to settle to a very small error is reduced. Second, the current-setting resistors, seeing only dc currents, do not influence the settling time and thus need not be high-speed resistors—wirewounds could be used for this purpose.

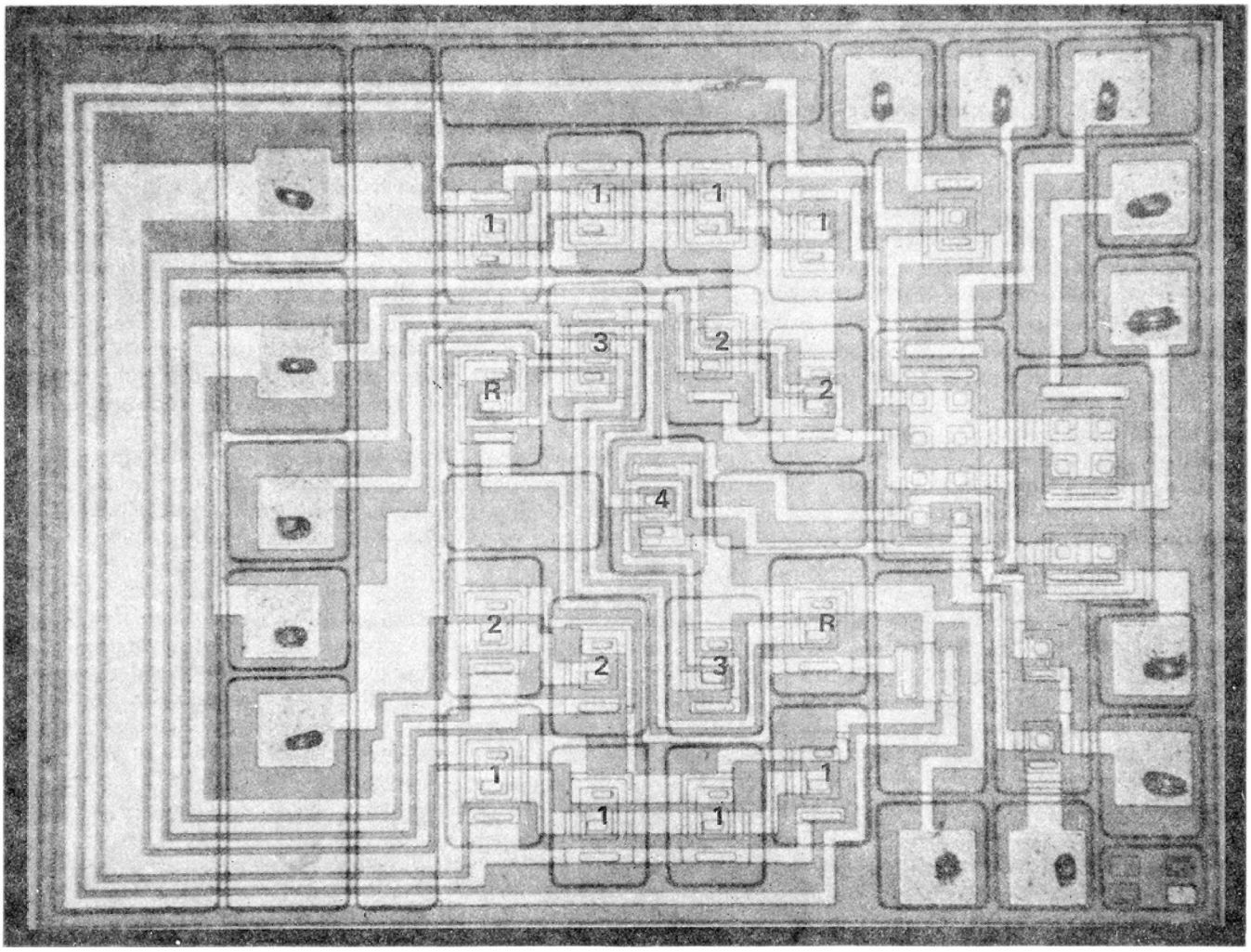
The speed of the bit switch is especially enhanced by the low parasitic capacitances resulting from dielectric isolation and the low common-base output capacitance, C_{OB}, of the bit-switch transistors. The time constant at the steering transistors' emitter is very short because of the low output capacitance of the current-source transistor and the low stray capacitances that result from the absence of connections to external circuitry.

The total output capacitance, which limits the speed of any current-to-voltage conversion following the switch, is exceptionally low—approximately 5 picofarads total for all eight collectors connected to the output point. The low output capacitance also permits the greatest bandwidth to be realized from broadband operational amplifiers in high-accuracy converters and with resistive terminations provides better rise times than had been previously possible. An added benefit of dielectric isolation is the low device-to-device leakage.

The chip geometry, which contributes heavily to the performance, is shown in Fig. 7. Unlike the chip previously described, a special arrangement of the current-source transistors is used to counteract the effects of

PROPERTIES OF D-A CONVERTER BIT SWITCHES

Configuration	Current switching or steering	TTL compatiblity	Resolution (bits)	Speed	Thermal tracking	Freedom from thermal tail	Compensation		Freedom from current leakage
							α	V_{BE}	
Diode-npn (Fig. 1)	Switching	Level shifted	10 – 11	Slow	Fair	Poor	No	Crude	Poor
Diode-pnp (Fig. 2)	Switching	Direct	10 – 11	Slow	Fair	Poor	No	Crude	Poor
pnp-pnp (Fig. 3)	Switching	Direct	10 – 11	Medium	Fair	Poor	No	Crude	Good
pnp-pnp ref. servo (Fig. 4)	Primarily switching	Direct	12 – 14	Medium	Fair	Poor	Yes	Fair	Good
Monolithic npn (Fig. 5)	Switching	Level shifted	12 – 14	Medium	Good	Fair	Yes	Precise	Fair
Monolithic pnp (Fig. 7)	Steering	Direct	16	Fast	Excellent	Excellent	Yes	Precise	Good



7. Current-steering geometry. Multiple-bit transistors are arranged symmetrically around geometric center so that gradients tend to average out—eight transistors for bit 1, for example, have same average temperature as four transistors for bit 2.

thermal gradients on transistor parameters.

The paralleled transistors used for each bit are arranged so that the geometric centers of all bits are coincident (the transistors are symmetrically arranged around the transistor for bit 4). This results in the elimination of thermal-gradient effects, whether internally or externally generated, since the average temperature for each group of bit transistors will be the same.

Thus, thermal tracking of the bits is substantially improved, and internally generated thermal tails are eliminated. The geometry of the chip results in thermal-tail values of less than 1 part per million of full scale for 3-mA full scale and 4 ppm of full scale for a full-scale output of 16 mA. Further, this geometry provides cancellation of diffusion gradients in any direction, resulting in excellent matching of α and V_{BE}.

The performance of d-a converters constructed with current-steering bit switches can exceed in accuracy, over wide temperature ranges without sacrificing speed, converters that are constructed with previously available switches. A 0.3-mV V_{BE} match, in combination with a 1% match in β, which are characteristic of the chip, permits the construction of d-a converters having a ¼-LSB linearity and 14- to 16-bit resolution when used with suitably accurate and trimmed resistors.

The contribution of the switches to the temperature coefficient of differential nonlinearity is primarily the result of a temperature-coefficient error in the dc match, which is 1 ppm/°C nominal. This value, when applied to converters, results in approximately 1 ppm/°C worst-case and ¼ ppm/°C typical differential nonlinearity.

The V_{BE} match of 2 μV/°C maximum will contribute only 0.1 to 0.3 ppm/°C error as differential nonlinearity (the V_{BE} match error will always be small, compared with the α-related error for bit-resistor voltages of 3 V or greater, but is more significant for a smaller voltage, such as 1 V). Output-current leakage totals 10 pA nominal and doubles with each +10°C. At 125°C, this is still only 1 ppm of full scale for a 10-mA full-scale converter.

The switching speed of a current-output d-a converter using the chip exceeds previous discrete or monolithic bit-switch designs, with 2- to 3-nanosecond rise time and typical settling times of 30 ns to within 0.1% and 60 ns to 0.01%. The low voltage and current errors permit the construction of micropower converters with full-scale output as low as 40 μA and bit-resistor voltages as low as 1 V or 1.5 V. A low-voltage converter can be assembled to operate from a single +5-V dc supply with performance comparable to units powered from ±15 V dc, but it will have a unipolar output current. □