charging rate, which makes the ujt emitter voltage increase at the same linear rate, regardless of the input voltage.

When the applied voltage is less than 70 volts rms, the ujt doesn't fire. In this case, the voltage across the load results from the voltage divider formed by R_1, D_5 and the load itself. This is represented by the lower corner of the regulation curve. The dashed part of the regulation curve indicates that the unijunction will fire randomly between 70 and 75 volts.

The value of R_2 is chosen to limit the ujt interbase voltage to less than 35 volts, its maximum rating. The zener voltage and R_3-C time constant control the firing angle. R_4 limits scr gate current.

The average voltage across the load can be adjusted by changing the value of R_1.

For the values shown, the voltage across R_2 is 30 volts d-c, ±1.5 volts, for line voltage varying from 100 to 200 volts a-c.

Matching gate potential to FET pinchoff voltage

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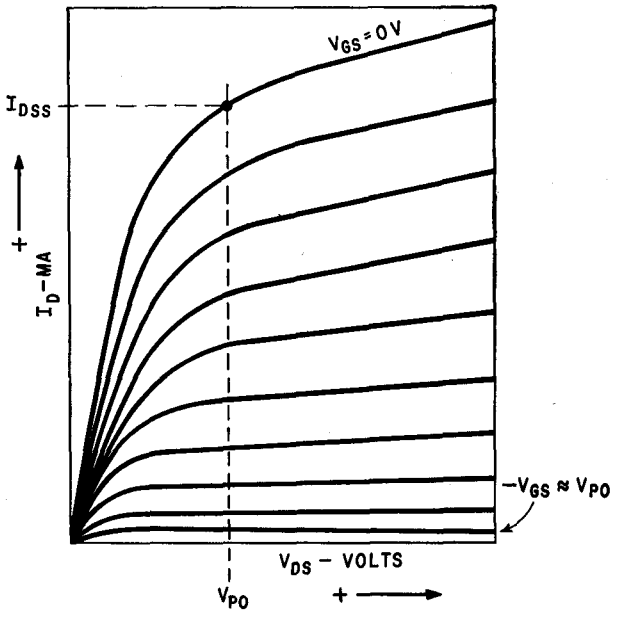
When an increase in a field-effect transistor's drain-to-source voltage causes little or no increase in drain current, the FET's pinchoff voltage has been reached. But it is not easy to determine this voltage, since it lies towards the end of the knee of the voltage-current curve. Direct measurement cannot obtain values for V_{PO} accurate to better than plus or minus one volt.

However, it is possible to find a gate voltage which is equal in value to the pinchoff voltage. The circuit at right shows how this gate voltage may be applied and measured conveniently.

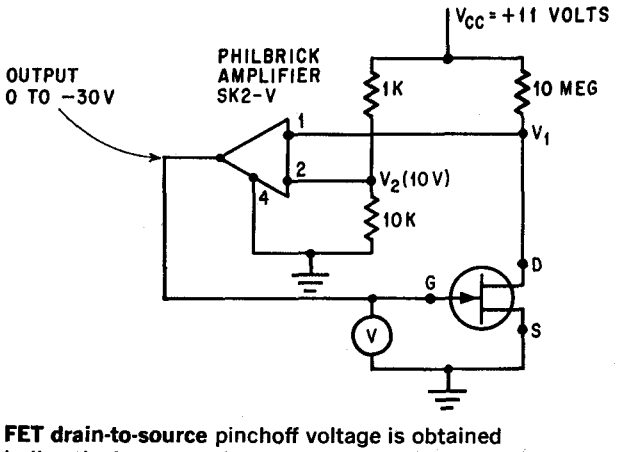
Analysis of the characteristic FET curves has shown that the gate voltage which holds drain current below 0.1 microamp is approximately equal to, though opposite in polarity from, the pinchoff voltage. Readout on a voltmeter connected from gate to ground gives a value which matches the pinchoff voltage.

When a FET is inserted in the circuit, the drain voltage V_1 approaches zero. The drain is connected to both the noninverting input of the Philbrick amplifier and a reference voltage V_2, which is connected to the inverting input of the amplifier. Since the drain is close to zero volts, the amplifier produces a negative output potential, which is applied to the gate of the FET under test, an n-channel type, turning it off.

When the amplifier input voltages are balanced, there is a voltage difference $V_{CC} - V_2$ across the 10-megohm drain resistor. The circuit is designed so that this voltage correponds to the magnitude of drain current change specified at V_{PO}. In this case, with $V_{CC} - V_2 = 1$ volt, $I_D = 0.1$ microamp.



Typical FET drain characteristics. V_{PO} is drain voltage that causes little or no change in I_D when $V_{GS} = 0_V$.



FET drain-to-source pinchoff voltage is obtained indirectly, by measuring gate-to-source voltage that causes $I_D = 0.1$ microamperes.

The pinchoff voltage of p-channel FET's can be measured by changing the polarity of V_{CC} and reversing the inputs to the amplifier.