TELEDYNE PHILBRICK

Application Note

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OPERATIONAL AMPLIFIER PARAMETER DEFINITION AND MEASUREMENT GUIDE

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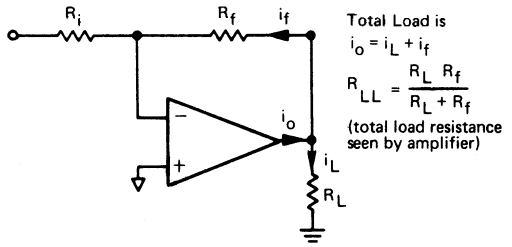
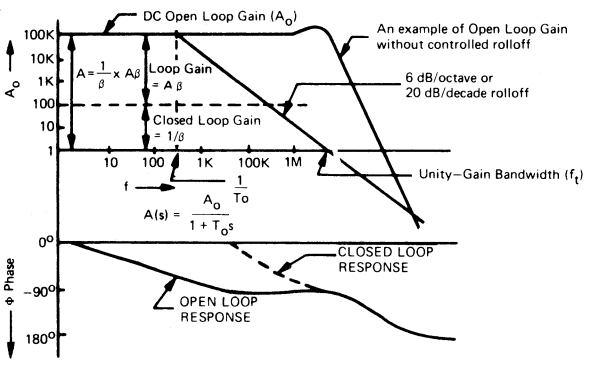
Commercially, the Operational Amplifier has been available for over 30 years (George A. Philbrick Researches was founded in 1946) and, for the most part, the meaning of the terms and specifications which describe them has been standardized and joined the jargon of engineers and scientists in all disciplines. However, it is often necessary for a user to know *exactly* what a manufacturer means by a particular parameter and, what is often more important, *how to measure it.*

This bulletin gives both expert and novice the fundamentals necessary to duplicate the test set-ups used by Teledyne Philbrick's Production Test and Quality Control Departments. Most of its content has been taken verbatum from the Teledyne Philbrick engineering document entitled "Operational Test Standards."

I Open Loop Gain, A_O

1. Open Loop Gain is defined as the ratio of the output voltage to the error voltage between the inputs.
2. A_O is a function of load resistance, temperature, frequency, power supply voltage, common mode voltage, and time (change in component values due to aging).
3. 

4. A_O is infinity for the ideal amplifier.
5. 

Operational Amplifier Typical Bode Plot

To calculate gain at different frequencies greater than or equal to the –3 dB point for **6 dB/octave rolloff only**, use:

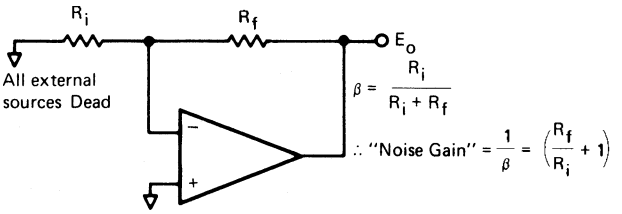
(gain) (frequency of interest) = (1) (unity gain bandwidth)

Condition for stability from Bode plot:

$\Phi < 180^o$ **AT** $A\beta = 1$

6. 12 dB/octave amplifiers –
   a. have a higher closed loop bandwidth
   b. are more difficult to stabilize
7. Loop gain ($A\beta$) is important for gain accuracy, gain stability, closed loop bandwidth, and effective output impedance.
8. β = that fraction of the output fed back to the input, "Noise Gain" $\equiv \frac{1}{\beta}$

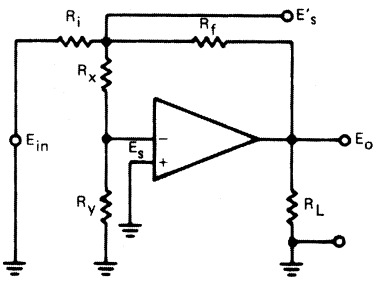
EXAMPLE:



9. Gain Error $\cong \frac{\text{"Noise Gain"}}{A_O} = \frac{1}{A\beta}$
10. Loop gain is equal to open loop gain divided by closed loop gain.

$$A\beta \cong \frac{A_O}{G_{CL}}$$

11. For 1% gain accuracy, make loop gain equal to 100X closed loop gain.
12. A_O test circuit
    Gain (A_O) at Full Rated Load



$R_f = R_i$ Full Rated Load = $R_{fl} = \frac{(R_L)(R_f)}{R_L + R_f}$

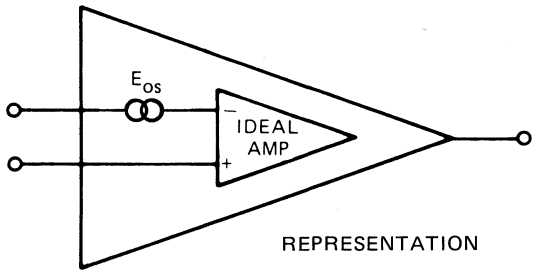
$A_O = \frac{E_o}{E_s}$

A Ratio of $\frac{R_x}{R_y}$ may be used to easily measure E_s

$E_s = E_s \frac{(R_y)}{(R_x)}$ $A_O = \frac{E_o (R_x)}{E_s (R_y)}$ $R_x \gg R_y$

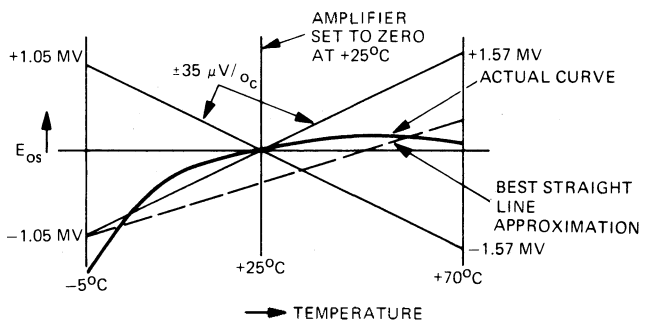
II Input Voltage Offset, E_{OS}

1. E_{OS} is defined as that voltage which must be applied to the input to obtain zero output with zero input signal. This specification is normally given referred to the input. E_{OS} is zero for an ideal amplifier. E_{OS} is the major source of error in low impedance circuits.

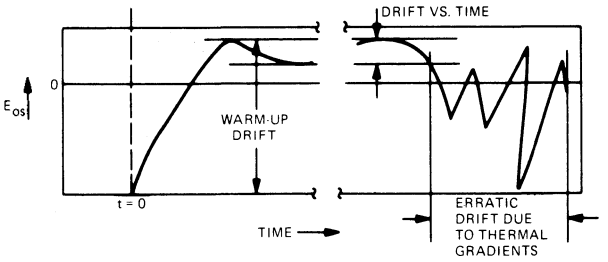


2. Initial E_{OS} is primarily determined by V_{BE} mismatch in the differential input stage and unbalance in the second stage attenuated by the gain of the first stage.
3. E_{OS} drift is a function of temperature, time, power supply voltage, and common mode voltage. Less obvious problems are due to thermal gradients causing differences in temperature between the two input devices (even two perfectly matched transistors with an individual $\Delta V_{BE}/\Delta T$ = 2.4 mV/°C will cause a ΔE_{OS} of about 24 μV if a thermal difference of 0.01°C exists), and self-heating due to rectification of high frequency overdrive signals because the base-emitter diode of a transistor is a rectifying junction.
4. E_{OS} vs Temperature is usually given in μV/°C and is a linear approximation of the slope of E_{OS} vs Temperature range. This indicates the degree of mismatch of the numerous stages of the amplifier. This specification is also given as a maximum deviation over the temperature range.

   To measure this parameter, the initial offset must be zero at +25°C. To emphasize this, if the initial offset is 1 mV at +25°C before measurement, then there will be an excess 3.3 μV/°C (for bipolar transistors) as a consequence of the initial 1 mV.
5. The time drift ($\Delta E_{OS}/\Delta t$) is specified at a constant temperature (usually +25.00 °C).
6. Chopper stabilized amplifiers, at present, have the best drift specifications and do not depend on drift cancellation; therefore, they are more immune to thermal gradients.
7. Typical $\Delta E_{OS}/\Delta T$

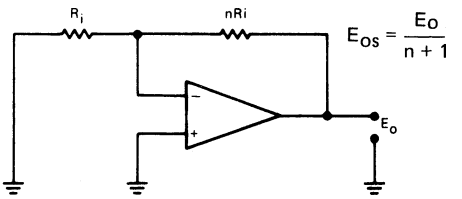


8. Typical $\Delta E_{OS}/\Delta t$



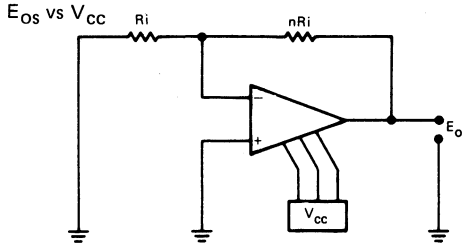
9. E_{OS} Test Circuits

Initial E_{OS} and E_{OS}TC



$$E_{OS} = \frac{E_o}{n+1}$$

E_{OS} vs V_{CC}



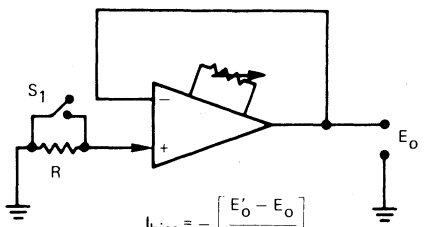
$$E_{OS} \text{ vs } V_{CC} = \frac{\max \Delta E_O}{\Delta V_{CC}\,(n+1)}$$

III Input Bias Current, I_{bias}, and Input Offset Current I_{OS}

1. I_{bias} is that current which flows in or out of either terminal under zero signal conditions. For transistor input amplifiers, this is the required base current of the input stage for proper operation. For FET inputs, this current is due to leakage, and is normally 3-4 decades better than transistor bias currents. For single-ended amplifiers, such as chopper stabilized amplifiers, this specification refers only to the negative input. I_{OS} is the difference between I_{bias} (−) and I_{bias} (+).

   Note: It should not be specified $\left(\frac{I_{bias}(+) + I_{bias}(-)}{2}\right)$
2. These are important parameters for high impedance circuits.
3. Both I_{bias} and I_{OS} are functions of temperature, time, power supply voltage, and common mode voltage.
   a. These parameters are specified as an average slope over a specified temperature range in nA/°C, similar to the voltage offset temperature coefficient. They are also specified as a maximum deviation over a defined temperature range. (This method makes interpolation over a limited temperature range difficult.)
   b. I_{bias} and I_{OS} vs time is specified at a constant temperature (usually +25.00 °C).

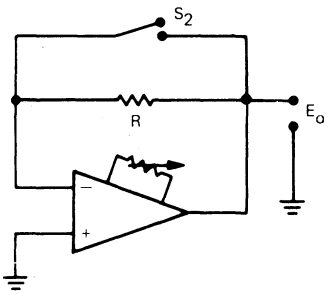
4. Amplifiers without internal bias current compensation will have a single polarity specification (i.e., +100nA) and amplifiers with internal compensation which will have a dual polarity specification (i.e., ±30 nA). The internal compensation can be resistors from the positive supply to each input, providing a bucking current (Note: This resistor may tend to lower the common mode impedance.) or a complex active device circuit (patented) which provides for compensation not only at room ambient but over the complete operating temperature range.
5. If bias current or offset current is a problem it is usually possible to find an amplifier with lower specified currents or current drift.
6. I_{bias}, I_{os} test circuits. I_{bias} (+) and (–) at 25°C.



$$I_{bias} = -\left[\frac{E'_o - E_o}{R}\right]$$

$E'_o = E_o$ with S_1 open

I Bias (+)



$$I_{bias} = +\left[\frac{E''_o - E_o}{R}\right]$$

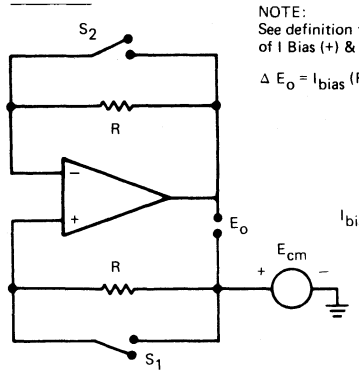
$E''_o = E_o$ with S_2 open

I Bias (–)

I_{bias} vs E_{cm}

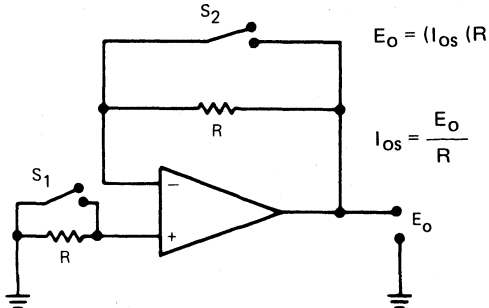
NOTE:
See definition for calculation of I Bias (+) & I Bias (–)

$\Delta E_o = I_{bias}(R)$



$$I_{bias\ vs\ E_{cm}} = \left\{\begin{array}{l}\dfrac{\Delta I_{bias}\ (+)\ max}{\Delta E_{cm}} \\ \dfrac{\Delta I_{bias}\ (-)\ max}{\Delta E_{cm}}\end{array}\right.$$

I_{os} $\quad I_{os} = (I_{bias}\ (-) - I_{bias}\ (+))$

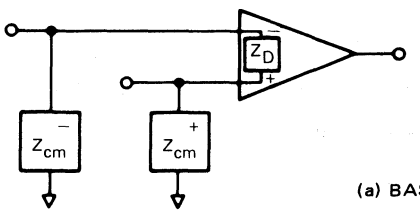


$E_o = (I_{os}\ (R)$

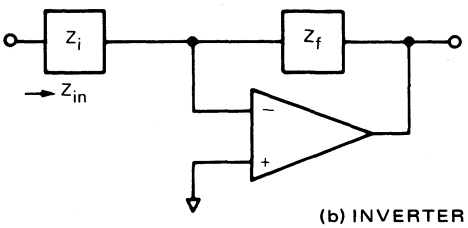
$$I_{os} = \frac{E_o}{R}$$

IV Input Impedance: Differential, Z_d; Common Mode, Z_{cm}

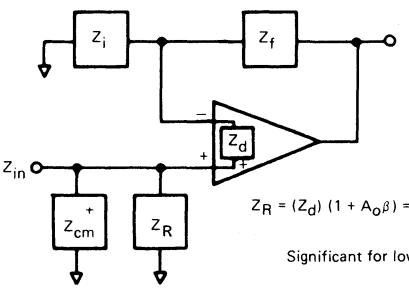
1. Z_d is the open loop impedance between the inputs of the amplifier and is specified in the active region as a parallel resistive and capacitive impedance. (Note: This makes the impedance frequency dependent.) This is the only impedance specified in single-ended input chopper stabilized amplifiers.
2. Z_{cm} is the impedance seen looking between either input and ground. This is also specified as a parallel resistive and capacitive component and Z_{cm} (+) and Z_{cm} (–) are assumed to be equal.
3. Representation



(a) BASIC OPEN LOOP



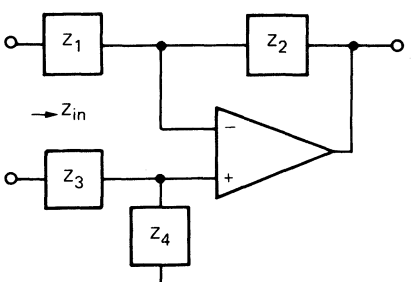
(b) INVERTER: $Z_{in} \cong Z_i$



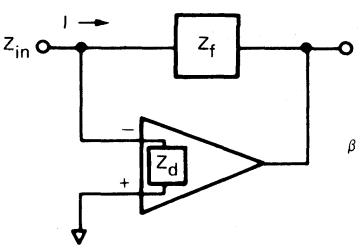
$$Z_R = (Z_d)\ (1 + A_o\beta) = Z_d\ (1 + \frac{A_o Z_i}{Z_i + Z_f})$$

Significant for low loop gain ($A\beta$)

(c) FOLLOWER WITH GAIN: $Z_{in} \cong Z_{CM} \parallel Z_R$



(d) DIFFERENTIAL: $Z_{in} \cong Z_1 + Z_3$



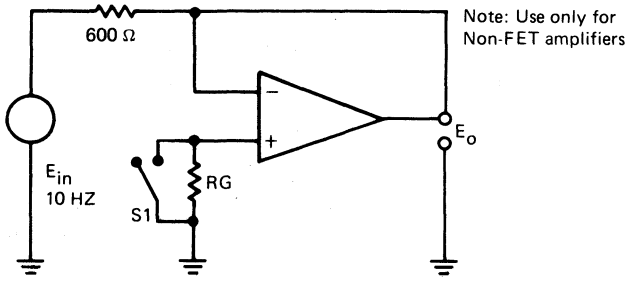
$$\beta = \frac{Z_d}{Z_d + Z_f}$$

(e) CURRENT AMPLIFIER: $Z_{IN} \cong Z_f / 1 + A_o\beta$

For $Z_f \ll Z_d$

4. The capacitive portion of input impedance becomes dominant at high frequencies. For wideband amplifiers with feedforward capacitance (the effective input capacitance is as large as 0.02 μF in this case), the response for the non-inverting connection will be limited to low frequencies. Amplifiers without feedforward capacitors will generally not have effective capacitances greater than 10 pF.
5. FET and varactor (parametric) input amplifiers generally have the highest input impedances. These impedances are in the range of 10^{11} to 10^{14} Ω. Transistor inputs in Darlington configurations have somewhat higher input impedances (2-6MΩ) than normal transistor input configurations (50K-500kΩ) due to the bootstrapping effect of this configuration.
6. Finite input impedance primarily reduces loop gain.
7. Z_d, Z_{cm} Test Circuits

Differential Input Impedance (Z_d)

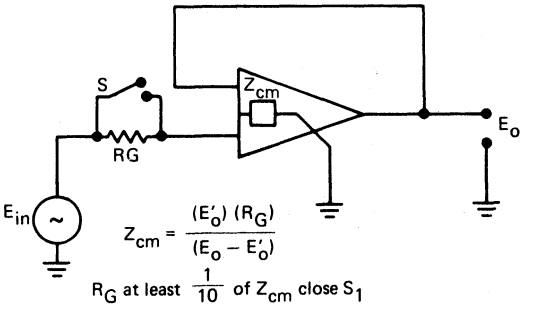


$$Z_d = \frac{(E_{out})\,R_g}{E_{out}' - E_{out}}$$

E_{out}' is E_{out} with S_1 open

NOTE: This measurement is not especially recommended as it is extremely difficult and delicate to measure.

Common Mode Impedance (Z_{cm})



$$Z_{cm} = \frac{(E_o')\,(R_G)}{(E_o - E_o')}$$

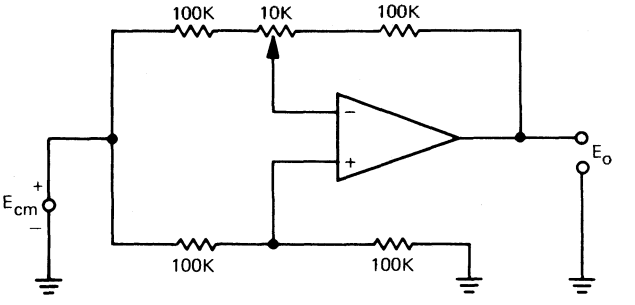
R_G at least $\frac{1}{10}$ of Z_{cm} close S_1

read E_o', open S_1 read E_o'

V Input Voltage Range

1. The Maximum Differential Input Voltage rating is the absolute maximum voltage which may be applied across the amplifier inputs without causing damage. This is primarily a function of the input transistor breakdown voltages and dissipation at the junctions.
2. The maximum (DC) common mode voltage (both inputs moving together as in a follower configuration) is the maximum voltage that may be applied to either input and ground without causing damage.
3. The usable common mode voltage is the maximum voltage from either input to ground that may be applied and still remain in the active (linear) region. The active region is sometimes measured with a distortion meter on the output and increasing the common mode voltage until the harmonic distortion reaches some arbitrary limit (1% to 3%).
4. Parametric (varactor) amplifiers will usually operate within specification with common mode voltages 5 to 10 times the power supply voltage.
5. E_{cm} Useful Range Test Circuit

E_{cm} Useful Range



VI CMRR, Common Mode Rejection Ratio

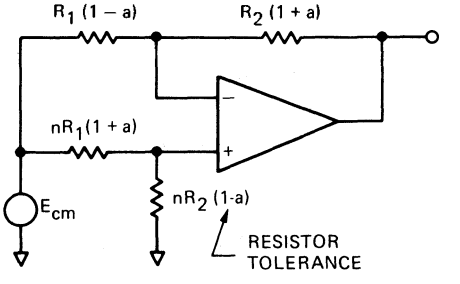
1. CMRR is the ratio of input common mode voltage to the error produced at the inputs by this common mode voltage. It is sometimes defined as the ratio of the open loop gain to the common mode gain, where common gain is the ratio of the output voltage to the common mode voltage.
2. CMRR is specified at DC and is frequency dependent. Manufacturers will sometimes supply curves of CMRR vs. frequency for applicable amplifiers.
3. CMRR is often nonlinear and poorer at the extremes of the common mode voltage swing.
4. CMRR is an important parameter for follower and differential configurations.
5. The circuit components also have a CMRR – see example below:

CIRCUIT COMMON MODE (NOT FOR AMPLIFIER)

$$CMRR_C \cong \left(\frac{\frac{R_2}{R_1} + 1}{4a}\right)$$

∴ TOTAL CMRR IS $CMRR_t = \frac{(CMRR_C)(CMRR_A)}{CMRR_C + CMRR_A}$

$CMRR_C$ = CIRCUIT CMRR $CMRR_A$ = AMPLIFIER CMRR

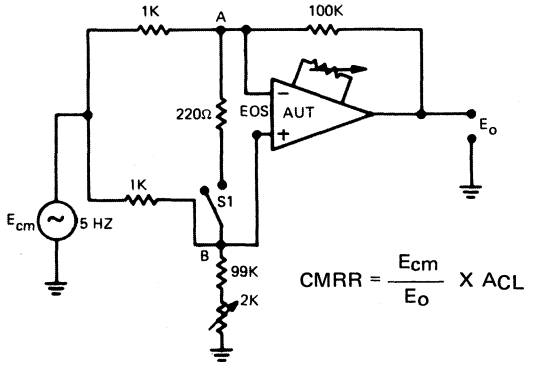


It is therefore necessary to trim the circuit resistors to minimize DC **circuit** CMRR such as rheostat in series with nR_2 (1–a). To minimize AC circuit common mode, a trimmable capacitor in parallel with nR_2 (1–a) could be used.

6. To calculate common mode error use the following equation:

$$\% \text{ error} = \left(\frac{E_{cm}}{CMRR} / V_S\right)(100)$$ (V_S = signal input magnitude) and add errors due to drift, source loading, long term aging and finite gain due to common mode error for the total error.

7. CMRR Test Circuit



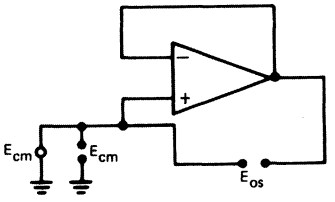
$$CMRR = \frac{E_{cm}}{E_o} \times A_{CL}$$

USE ONLY FOR $A_O >> CMRR$

NOTE: (1) With amplifier out, S_1 open and E_o shorted to ground, set E_{cm} = 15V, adjust 2 KΩ resistor for 0 ± 10μV between points A, B.

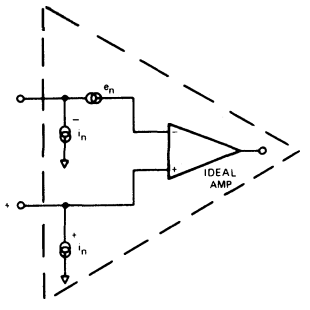
(2) Ground E_{cm} and adjust E_{os} to 0 ± 1 mV at the output, then CMRR = (Δ E_{cm}/ Δ E_o) X 1000. CMRR is averaged over the total E_{cm} range unless otherwise specified.

(3) For CMRR < 60 dB or A_V < 10K, open S_1 for A_{CL} = 100.



VII Input Voltage Noise, e_n, and Current Noise, i_n

1. e_n is the output voltage noise which has been referred to the input of the amplifier. Note that E_{os} drift may be considered to be a form of very low frequency (< 0.1 Hz) noise voltage and therefore e_n can be considered to be analogous to ΔE_{os} except for its frequency spectrum.
2. i_n is the noise current flowing in either of the amplifier inputs. Note that input offset current drift may be considered to be a form of very low frequency noise current.
3. Representation:



4. Both e_n and i_n can be expressed in terms of RMS or peak to peak, but bandwidth must always be defined. Note: the ratio between peak to peak and RMS is approximately 5:1.
5. There are many sources of noise including hum, flicker, drift, chopper spikes, thermal, signal, and coupling.
6. Many types of noise exist:
   a. Shot Noise is random electron emission. In vacuum tubes it is from the cathode, whereas in semiconductors it is the random diffusion of minority carriers and random generation and recombination of hole-electron pairs.
   b. Thermal noise is the random motion of free electrons. It is also called white noise (in all frequencies) and a constant power density spectrum is assumed. In the case of resistors, thermal noise is called Johnson noise and this is one of the most important parameters to consider for a circuit other than the amplifier noise.

   To calculate Johnson Noise:

$$e_j = \sqrt{4\,k\,T\,(BW)\,(R)}$$

Some examples are at 23°C:

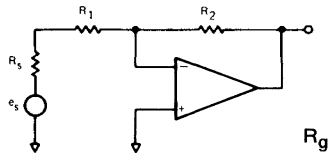
	R	BW	E_j
k = Boltzmann's constant = 1.38×10^{-23} joules	1 kΩ	60 kHz	1 μV rms
T = ° Kelvin absolute	100 kΩ	60 kHz	10 μV rms
BW = Bandwidth of interest (Hz)	10 kΩ	31 kHz	2.2 μV rms
R = Resistance (ohms)	100 kΩ	31 kHz	7 μV rms

   c. 1/f noise is a low frequency flicker noise due to surface conditions in semiconductors which has a power density spectrum proportional to 1/f. This is valid up to approximately 1 kHz and rises about 6 dB/octave.
   d. Popcorn noise is a recent discovery and is a low frequency step fluctuation most often encountered with integrated circuit operational amplifiers and probably arises in surface states where the transition region of the emitter base junction intersects the silicon surface.
7. For 6 dB/octave amplifiers, the effective noise bandwidth is $(\frac{\pi}{2})(f_{3dB})$.
8. When measuring noise with an average responding meter, add about 11% to account for the difference between the average rectified value of sinusoids (for which meter is calibrated) and RMS for white noise.
9. Noise specifications are most often given as input noise for zero source impedance. The equivalent input noise at other impedances is:

$$E_N = \sqrt{e_n^2 + (i_n \times R_g)^2 + e_j^2}$$

amplifier noises (RMS) Johnson Noise

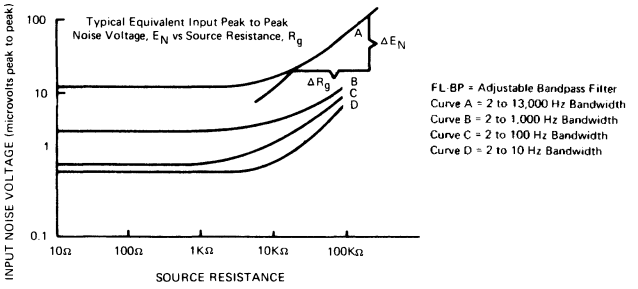
EXAMPLE: To Find R_g (Equivalent source resistance)

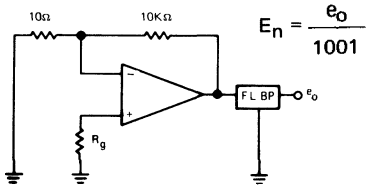


$$R_g = \frac{(R_s + R_1)\,R_2}{R_s + R_1 + R_2}$$

Note that noise current will flow through the feedback resistor, buts its effect at the output is negligible due to the choice of the 10 KΩ feedback resistor. The noise current can be calculated from the approximate slope of the "equivalent" input noise voltage curve.

$$i_n = \frac{\Delta E_n}{\Delta R_g} \text{ if } i_n R_g \gg e_n$$





$$E_n = \frac{e_o}{1001}$$

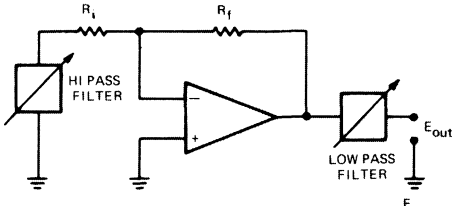
10. Noise figure is the ratio in dB of equivalent input noise power of the amplifier with given source resistance divided by the noise power generated in R_g alone = $20 \log_{10} (\frac{E_N}{e_j})$.

11. Amplifiers which exhibit low e_n generally have high i_n and vice versa.

12. e_n, i_n Test Circuits

Input Noise Voltage

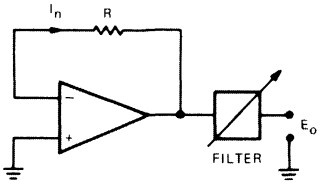
Two regions of noise will be specified: 1/f (0.16 Hz to 1.6 Hz) and wideband (0.16 Hz to 16 kHz) or as specified.



$$E_{noise} = \frac{E_o}{\frac{R_f}{R_i} + 1}$$

Input Noise Current

The two ranges will be 1/f noise (0.16 Hz to 1.6 Hz) and wideband noise (0.16 Hz to 16 kHz) or as specified.



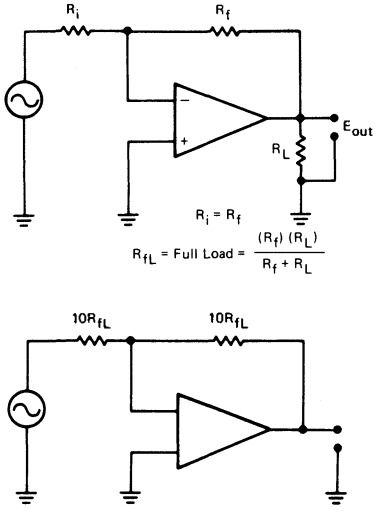
$$I_n = \frac{E_o}{R}$$

VIII Frequency Response

1. Frequency for Full Output, f_s, f_p

f_s is the maximum frequency for "undistorted" output (maximum sine power out 3% to 5% distortion), whereas f_p is frequency for full peak to peak output normally measured with a triangle wave input. These are large signal characteristics and are not the –3 dB point of the open loop gain curve.

f_s, f_p Test Circuit:

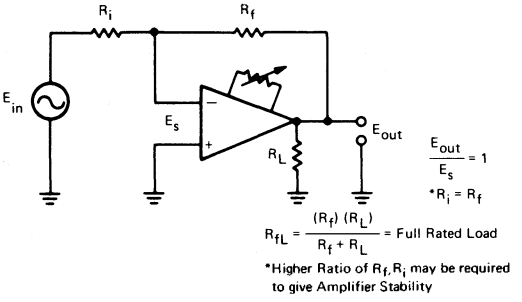


Frequency increased until 5% distortion appears at output

2. Unity Gain Bandwidth, f_t

This is the frequency at which the open loop gain of the amplifier is one. f_t is a point of interest for "tight fedback" configurations. This is a small signal characteristic.

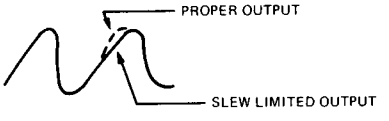
f_t Test Circuit:



E_o = 50mV P-P or as specified

3. Slew Rate

Slew rate is the ability of the amplifier to produce large, rapid changes in output voltages. For linear IC amplifiers, this is a direct function of the compensation capacity.



Slew rate is related to f_S by the following relation:

$T_R \approx \frac{0.35}{f_S\,(mHz)}$ μsec = Rise time for full p-p output voltage swing.

Since slew rate $= \frac{dV}{dt}$

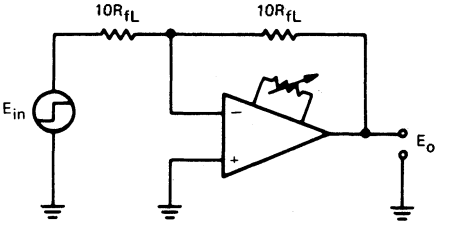
$$\frac{dV}{dt} = \frac{V_{out}\,(Volts\ p\text{-}p)}{T_R} \approx \frac{f_S\,(mHz) \times V_{out}}{0.35} = V/\mu s$$

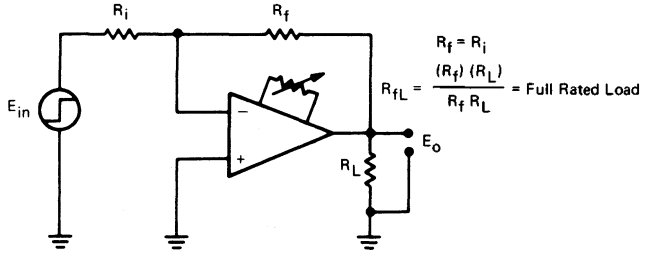
Be careful of output load capacitance causing a slew limit (in addition to amplifier slew rate) since:

$$\frac{dV}{dt} = \frac{i_{out}}{C_L}$$

Slew Rate Test Circuit:

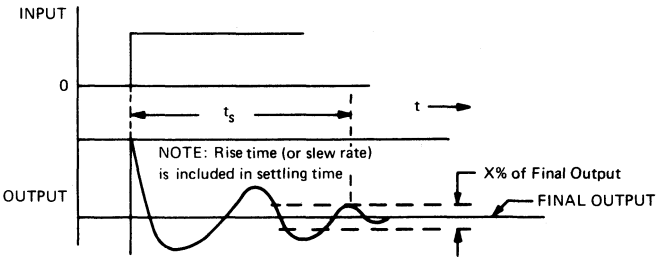
Slew Rate is the maximum time rate of change of output voltage for a step input measured from the 30% to 70% points on the output wave form. The output is driven from full negative to full positive output and vice versa.





4. Settling Time, t_S

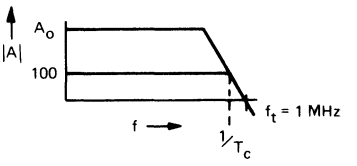
Settling time is the time from application of a step input to the time for the amplifier's output to recover to within a symmetrical specified percent of desired final output. Note: the time and desired percent of output, referred to output, must be specified. If settling time is referred to input, the output may still be moving even though the summing point voltage has settled, because of parasitics in the feedback, miller capacitance still charged by currents, and "thermal tails" generated in the amplifier by the pulse. These "thermal tails" are particularly important when sub-microsecond settling time to 0.01% is being specified. In this region it is impossible to calculate t_S from other device parameters. IT MUST BE MEASURED! (see TP 1430 data sheet)

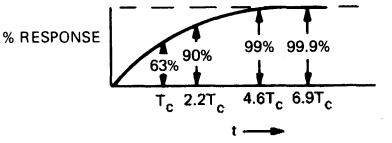


For 6 dB/octave amplifiers, the settling time is fastest for a gain of one, and longer for higher closed loop gains.

Transient Response

If one has a closed loop gain of 100 and wishes to calculate the time for an amplifier to reach 0.1% of final output from a step input, use the following:





$$T = 6.9\,T_c \quad \frac{1}{T_c} = \omega_c = \left(\frac{f_t}{1/\beta}\right) 2\pi = \frac{(1MHz)\,(2\pi)}{(1/100)}$$

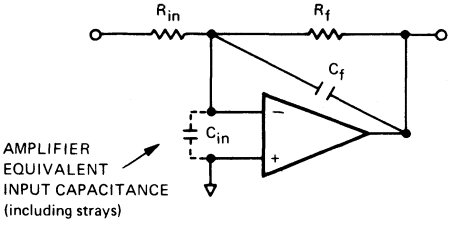
$1/\beta$ = CLOSED LOOP GAIN

$$T = 6.9\,T_c = 6.9\ \frac{(100)}{(6.28)(10^6)} = 110\,\mu sec$$

For Optimum Stability and Non-overshooting Response: Make the input time constant equal to the feedback time constant

$$R_{IN}\,C_{IN} = R_f\,C_f \text{ or } C_f = \frac{R_{IN}\,C_{IN}}{R_f}$$

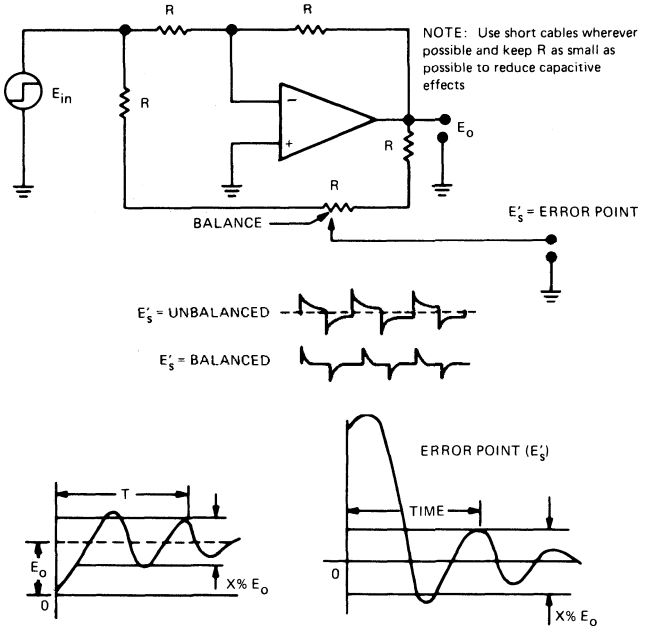
Some C_f should always be present whether it be parasitic or fixed component.



Note: You cannot extrapolate 0.01% settling time from 0.1% settling time.

– Settling Time Test Circuit:

Settling time is measured by balancing E_S' and measuring the time it takes E_S' to settle within .1% of E_O. Measure both the rise and the fall time.



5. Overload Recovery, T_{OL}

Overload recovery is the length of time required for an amplifier to return to its active region after being driven completely into saturation. Sometimes the stipulation is included that recovery will be to within some percent of full swing.

Overload recovery will generally be longer for impedances of 50 kΩ or greater.

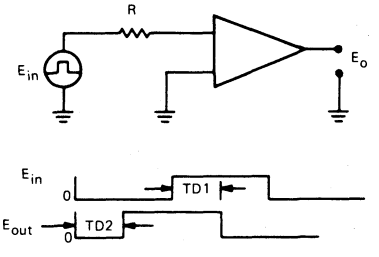
An output bound or clamp circuit to prevent amplifier saturation will improve overload recovery. A bound circuit is recommended especially for chopper stabilized amplifiers (with 60 Hz chopper drive) since overload recovery is quite long due to the large demodulator filter time constant.

For most amplifiers, overload recovery is comparable to $\frac{10}{f_S}$, where f_S is the frequency for full output with no visible distortion (5%).

Overload Recovery Test Circuit:

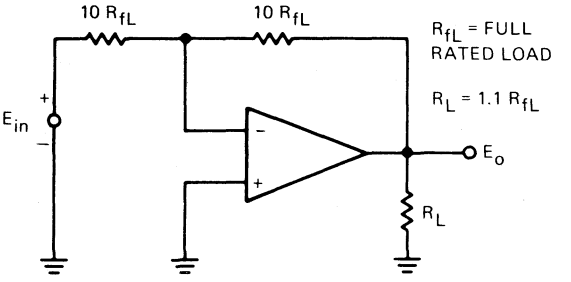
Recovery from Overdrive

E_{in} is set at 1/2 common mode voltage range or as specified.



IX Output Voltage and Output Current Rating, E_O, I_O

1. The E_O rating describes the peak output voltage referenced to zero without clipping and symmetry is usually implied.



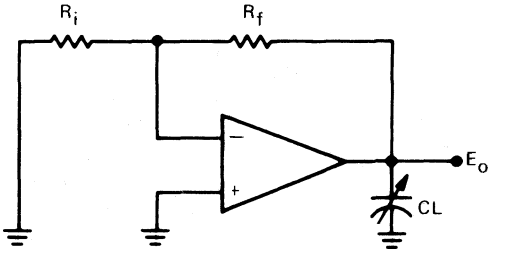
2. The quiescent power supply current, $\pm I_{CC}$, is the current required from the power supply when E_O is zero. Full output current is the sum of the quiescent and the output current, I_O.

X Storage and Operating Temperatures

1. The maximum operating temperature range indicates the minimum and maximum temperature to which the amplifier may be subjected without excessive deviation from the electrical specifications. A typical operating range is –25 °C to +85 °C with higher ranges for premium and MIL type amplifiers.
2. The maximum storage temperature range may not be exceeded without causing damage (catastrophic or permanent degradation of performance). Typical ranges are –55 °C to +100 °C with higher ranges for premium and MIL type amplifiers.
3. The gray area between operating and storage temperatures will be for degraded specifications which are sometimes given.

XI Capacitive Load

1. The capacitive load is the maximum capacitative load which the amplifier can drive without becoming unstable with specified input and feedback resistors with C_L initially 50 pF.



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